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# RESEARCH ON LOW TEMPERATURE, DIRECTED ENERGY PROCESSING OF VERY LARGE SCALE INTEGRATED STRUCTURES



ANTON GREENWALD
(617) 275-6000 EXT. 228

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The goal of this research program is to demonstrate processing techniques which can eliminate the need for high temperature thermal cycling of silicon wafers in fabricating very large scale integrated (VLSI) devices. Maintaining low temperatures for all processing reduces plastic deformation, diffusion and autodoping problems which would limit the application of submicron geometry design rules. Pulsed electron beam surface heating of the top micron of material is being investigated for annealing of ion-implantation damage and epitaxial regrowth of low temperature chemical-vapor-deposition (CVD)

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polycrystalline silicon films. Initial research has demonstrated the epitaxial regrowth of 0.3 micron films deposited at 800°C. Annealing of ion-implantation damage typical of buried layer applications has also been demonstrated. Effective uniformity of processing has been improved to ±4 percent in one (electron beam) pulse covering the surface of a 3-inch-diameter wafer. Research planned in the next 6 months will stress lower deposition temperatures and pulsed nonmelting techniques for annealing implantation damage. The program is about 2 months ahead of schedule.

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# REPORT SUMMARY

## 1.1 TASK OBJECTIVES

The goal of this program is to reduce the maximum temperature used in processing large scale silicon integrated circuits. Specifically, the program is to demonstrate: (1) that a thin silicon film can be deposited with impurity levels consistent with that required for active devices, (2) that this film can be changed to epitaxial crystal structure through pulsed irradiation by electron beams, (3) that ion-implanted junctions in this film or the substrate can be annealed by pulsed technology, and (4) that an operational device typical of very large scale integrated (VLSI) technologies can be fabricated by these techniques.

## 1.2 TECHNICAL PROBLEMS

Existing technology for the fabrication of integrated circuits uses high temperatures (over $1000^{o}C$) for the growth of epitaxial films and annealing of ion-implant damage. Plastic deformation of the substrate and diffusion from previously deposited layers occurs at these temperatures, but the effect is not limiting until the device size shrinks to submicron design rules. This program is to demonstrate that diffusion from the buried layer into thin epitaxial layers can be controlled and that active device junctions formed by ion-implantation can be annealed without intolerable distortion or diffusion of fine line, multiple layer geometries.

## 1.3 GENERAL METHODS

High temperature furnace processing steps are replaced by pulsed electron beam surface heating. Through control of beam fluence and particle energy this electron beam is used to heat, or to melt, 0.1 to 3.0 microns of silicon, heating the bulk of the substrate no more than 2 to $10^{o}C$. Short period thermal gradients cause epitaxial crystal regrowth in the heated surface material to anneal ion-implantation damage and recrystallize deposited films. Combined with a low temperature deposition technique to put down an appropriate film, the technique described can form an epitaxial film without defects over a patterned buried layer. To anneal ion-implanted junctions for small scale active devices, a nonmelting technique will be developed based upon multiple pulses of a low fluence electron beam.

## 1.4 TECHNICAL RESULTS/CONCLUSIONS

Excellent pulsed epitaxial regrowth of 0.3 micron chemical-vapor-deposition (CVD) polycrystalline silicon films was demonstrated. These films were deposited at 840°C, from silane without dopant added, onto (100) and (111) 0.003 ohm-cm arsenic doped substrates to simulate deposition on top of a buried layer. These thin films, and 0.5 micron conventional CVD epitaxial films, show that autodoping during CVD has occurred — implying that deposition temperatures must be reduced further. Samples were irradiated with a pulsed electron beam between 0.6 to 1.0 $j/cm^2$. The results are shown in Figures 3-6 and 3-7 in Section 3. An irregular surface of polycrystalline material was melted and changed to nearly flat, single crystal material oriented with the substrate. The doping profile of this film shows a sharp "corner" consistent with the solid-liquid regrowth model (see Figure 2-6). The dopant concentration in the film decreases rapidly to the uniform deposition level. Analytical modeling predicts controllable doping levels.

Most work on annealing ion-implantation damage was to develop a low fluence, rapid rate pulsed electron beam to demonstrate solid-phase annealing. The initial set of samples (see Section 4-4) shows that 100 pulses below melting thresholds will not cause diffusion of the implanted dopant profile. Regrowth of the crystal structure is incomplete and the amorphous material turned polycrystalline. Annealing with liquid phase techniques shows that the fluence of the beam must be increased more than 50 percent to melt crystalline material compared with amorphous material. The uniformity of processing, measured with pulsed annealing of high dose implants, is $\pm 4$ percent from the standard deviation of sheet resistance measurements across a 3-inch wafer.

## 1.5 IMPLICATIONS FOR FUTURE STUDY

Since CVD at 840°C has shown autodoping effects, films will be deposited at lower temperatures using infrared heated reactors and low-pressure chemical vapor deposition (LPCVD). Liquid phase annealing of buried layers will be studied in conjunction with pulsed epitaxy (see Table 1-1). Solid phase annealing studies will continue using higher fluence beams and a larger number of pulses.

TABLE 1-1. PRINCIPAL EXPERIMENTAL MATRIX FOR JULY - SEPTEMBER 1979

| Substrate Preparation | LPCVD |
|---|---|
| Not implanted | Amorphous |
| Implant Pulse Anneal | Polycrystalline |
| Implant Furnace Anneal | |

Note: This table shows the six types of samples which will be pulsed for epitaxial regrowth of the film and analyzed for crystal structure, implanted dopant profile, impurities, and defects. Substrates are 1-ohm-cm, (100), 3-inch o.d. float-zone silicon.

# SECTION 2
# SILICON FILM DEPOSITION

## 2.1 OBJECTIVE OF TASK 1

The objective of this task is to deposit on a silicon substrate a silicon film at low temperatures of high purity and appropriate doping and structure for Task 2, pulsed epitaxy. Additionally, high temperature, conventional, CVD epitaxial films will be deposited for comparison. All films are to be characterized for structure, doping profiles, and impurities or defects.

In this context, low temperature implies that the wafer is not heated to the point where plastic deformation or thermally induced stress will alter the geometry or relative position of the substrate or any film on its surface.[1] Also, the temperature must be kept below the point where diffusion of dopants occurs for a distance equal to the minimum line width (about 0.25 micron) or layer thickness. As a start, 800°C was used as the maximum permissible substrate temperature.

These deposited films are to be turned into crystal silicon used for active device structures. Therefore, the level of impurities is expected to be less than $10^{12}/cm^3$. Appropriate doping levels would be about 1 to 10 ohm-cm. The crystal structure before epitaxial regrowth is not critical, and part of the research on Task 2 is to determine what is the best stoichiometry for the deposited film. It was initially assumed that small grain poly or amorphous material would be preferred.

## 2.2 PLASMA ION DEPOSITION

On a program funded by Electric Power Research Institute (EPRI)[2], a facility for plasma ion deposition was constructed at Spire Corporation for research on thin film solar cells. No ARPA funds have or will be used in the construction of this equipment; however, with permission, it is being made available to this program. After a period of debugging, films for pulsed epitaxy experiments have been deposited and are now being characterized.

Films can be deposited in one of two ways: (1) through a plasma formed by electron beam bombardment of a silane gas source with the plasma partially confined by a magnetic field, or (2) through a low-density commercial ion beam source.[3] In both cases the substrate temperature can be independently controlled and will be kept below 600°C. Some films from the ion source have been partially analyzed. They are 1 to 3 microns thick. No significant difference in deposition over bare silicon or over a few thousand angstroms of oxide on silicon has been observed. A reflected electron diffraction pattern, Figure 2-1, shows small grain polycrystalline silicon plus an unidentified component believed to be a silicon oxide. One film was pulsed and blown off the substrate.

This experiment demonstrated that 1 to 3 micron small-grain polysilicon films can be deposited very rapidly up to 1 micron/minute, by this technique. The uncertain additional component must be eliminated for good electrical properties and pulsing characteristics (i.e., contamination can reduce adherence and cause the film to blow off the substrate when melted).

## 2.3 LOW TEMPERATURE CVD

For Task 2, small grain randomly oriented polycrystalline (or amorphous) silicon films are desired for analysis and comparison (after pulsing) to good quality epitaxial films. These films can be put down by low temperature chemical vapor deposition. The reactor available at Spire Corporation is an Applied Materials AMV 800. It was designed for epitaxial film growth, rather than poly, and has a minimum deposition temperature of about 840°C and cannot operate in the low pressure mode.

Previous attempts[4] at depositing polysilicon in this reactor have shown that noncontinuous films result from using chlorine-silicon compounds. Continuous films were achieved at 840°C from silane in hydrogen or nitrogen carrier gas. Randomly oriented, small grain poly was put down in nitrogen but not without some nitride contamination. For purity, initial CVD was restricted to $SiH_4$ in $H_2$ carrier gas with no added dopant. These films tend to be highly aligned polycrystalline[4,5] in the (100) orientation, which has the preferred, or faster, growth rate.

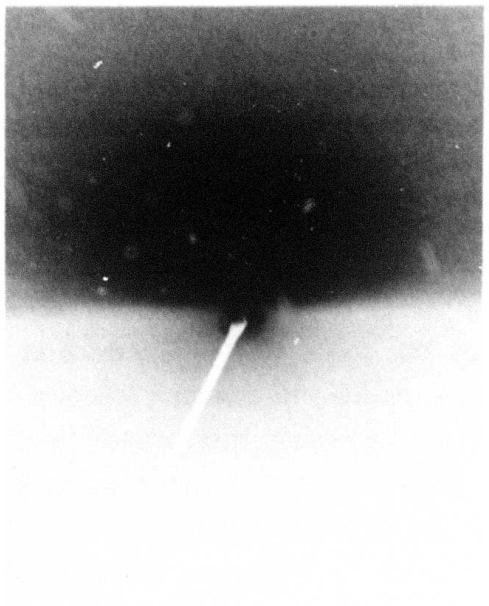


FIGURE 2-1. RHEED PATTERN FROM PLASMA ION DEPOSITED FILM SHOWING SMALL GRAIN POLYCRYSTALLINE SILICON DEPOSIT PLUS ADDITIONAL CRYSTALLINE COMPONENT NOT IDENTIFIED

Initial films were nominally 0.2 and 0.5 micron thick deposited on (111) and (100), highly doped (0.003 ohm-cm arsenic) substrates. This was done to simulate a deposit on a buried layer without having to implant or diffuse such a layer. Also, it provided sufficient dopant concentration to use secondary ion mass spectroscopy (SIMS) to determine the doping profile in as-deposited poly. Finally, it provided a test of the junction abruptness which could be achieved with pulsed epitaxy.

A final variation of substrate preparation was oxide etching in the reactor. All wafers were cleaned in HF to remove oxides just prior to insertion into and evacuation of the reactor. It is estimated that the time in air (less than 5 minutes) is sufficient to grow an oxide only 15A thick. In the reactor, the normal procedure for epitaxial deposition is to etch this thin oxide off the substrate at $1200^{o}C$ using a short time exposure to chlorine compounds (i.e., HCl etch). This is a high temperature processing step, and it was skipped on the sample runs labeled "no etch". Since removal of the contaminant oxide could be important for electrical properties, although the expected concentration in the film would be small (about $10^{12}/cm^{2}$ of film surface), the oxide was etched off in most films. Note that high temperatures before film deposition are not considered so damaging as the same temperatures during deposition because stress and deformation of the film surface can occur when cooling.

The film thickness was measured by a stylus instrument, DEKTAK,[6] and by cutting a shallow groove and staining. Initial CVD runs contained one wafer with a quartz chip to provide a step for absolute thickness measurement. However, deposits near the chip were not the same as on a smooth surface, and the measurement was not consistent with other diagnostics. To correct for this situation, CVD runs where films were deposited without etching of the oxide were made with one extra sample, a silicon chip having a thick (0.5 micron) oxide coating. Assuming film deposition did not vary over thin (15A) or thick (0.5 micron) oxides, etching the poly film on the extra sample over the thick oxide provided a step for accurate DEKTAK measurements. Other films, deposited with oxide etching, could not be measured this way, since an oxide coated chip ruined the deposition run when an etching step was included. One sample from all CVD runs was grooved by a diamond wheel and stained. Since the stain affects the dopant, it provides an optical differential delineating the junction region of the undoped poly and highly doped substrate. Motion or diffusion of the dopant would introduce a systematic error towards thinner films. The films prepared, substrate combinations, and thickness measurements are listed in Table 2-1.

TABLE 2-1. CVD FILMS FOR TASK 1

| Type | Sub-strate | I.D. No. | Deposition | | Measured Thickness (microns) | | | Comments |
|---|---|---|---|---|---|---|---|---|
| | | | Temp. (°C) | Time (Min.) | DEKTAK | Groove & Stain | C-V (minimum) | |
| Epi | (111) | 1467 | 1050 | 26 sec | 0.09 | 0.03 | 0.14 | polished |
| Epi | (111) | 1468 | 1050 | 1.0 min | 0.12 | 0.40 | 0.32 | polished |
| Epi | (111) | 1470 | 1050 | 2.0 | 0.25 | 0.69 | 0.58 | polished |
| Epi | (111) | 1471 | 1050 | 6.0 | 1.1 | 2.22 | 1.8 | polished, also 2.45 $\mu$m by spectrometer |
| Poly | (111) | 1499 | 840 | 3.20 | — | 0.12 | — | polished(1) |
| Poly | (111) | 1502 | 840 | 8.20 | — | 0.28 | — | polished(1) |
| Poly | (111) | 1503 | 840 | 8.20 | — | 0.29 | 0.13 | dull gray, non-uniform, (most data from this lot) |
| Poly | (100) | 1971 | 840 | 13.5 | 0.42 | 0.45 | — | polished, no oxide etch |
| Poly | (100) | 1974 | 840 | 15.0 | 0.36 to 0.43 | 0.19 | 0.25 | dull grey, non-uniform, |
| Poly | (100) | 2035 | 840 | 15.0 | — | 0.42 to 0.61 | — | polished, Kikuchi lines in RHEED? |

(1) tweezer marks visible.

Notes:

- Original epi thickness (specified) was 0.2, 0.5, 1.0, and 3.0 microns.
- Actual epi thickness estimated at 0.2, 0.6, 0.9, and 2.5 microns.
- All C-V thickness is minimum, nominally half actual value.
- Variations in measurements are discussed in text.
- All substrates 0.003 ohm-cm arsenic doped.

Initial visual observation of these films distributes them into two different sets: Those which are highly reflective and appear optically smooth through a microscope (Figure 2-2(a)) and those which appear to be dull gray, are nonreflective, and appear "grainy", through a microscope at 1000X (Figure 2-2(b)). All epitaxial films and some poly films deposited without etching the oxide were reflective. Most poly films were grainy or cloudy. Without the etch, also easily visible, were "decorations" near the edge of the wafer attributed to tweezer marks. The oxide etch in the reactor is a cleaning procedure and wafer handling without this step is critical.

At higher magnification, in a scanning electron microscope (SEM), the grainy or cloudy surface is covered by pyramid crystallites and more random raised features, all about 0.5 micron high and wide, as shown in Figure 2-3(a).[7]. Also visible in Figure 2-3(b)[8] are flat structures of roughly hexagonal shape which suggest grain boundaries. The SEM microphotographs are from the one sample in lot 1503 which was pulsed and analyzed most thoroughly.

Electron channeling analysis[7] was attempted. The key result is that the poly films were too highly aligned in one direction, or the technique not sensitive enough, to detect any difference between the pattern from good CVD epitaxial films and polycrystalline films as shown in Figure 2-4(a) and (b). To test the analysis, a series of amorphous silicon films were prepared by evaporation at $10^{-6}$ torr. The thickness was varied from 720 through 2500A. Electron channeling was blocked by the thinnest film. Since the CVD poly was over 3000A (0.3 micron) thick, this confirms that the deposit was strongly oriented in the (100) direction.

The polysilicon films were analyzed by reflected high energy electron diffraction[7] (RHEED) for crystal perfection. The technique only analyzes the surface to a depth of approximately 100A. However, if the surface has single crystal long range order, then the remaining part of the film must be the same. The technique can verify complete epitaxial regrowth from the substrate, but not partial regrowth or good epitaxy with thin surface layer damage. The electron beam used has a radius of about 25 microns and scans an area of 3 to 4 mm on a side. This is sufficient to differentiate between large grain poly and single crystal material. Also, from Figure 2-3, the grain size is less than 0.5 micron and this should be readily distinguished.

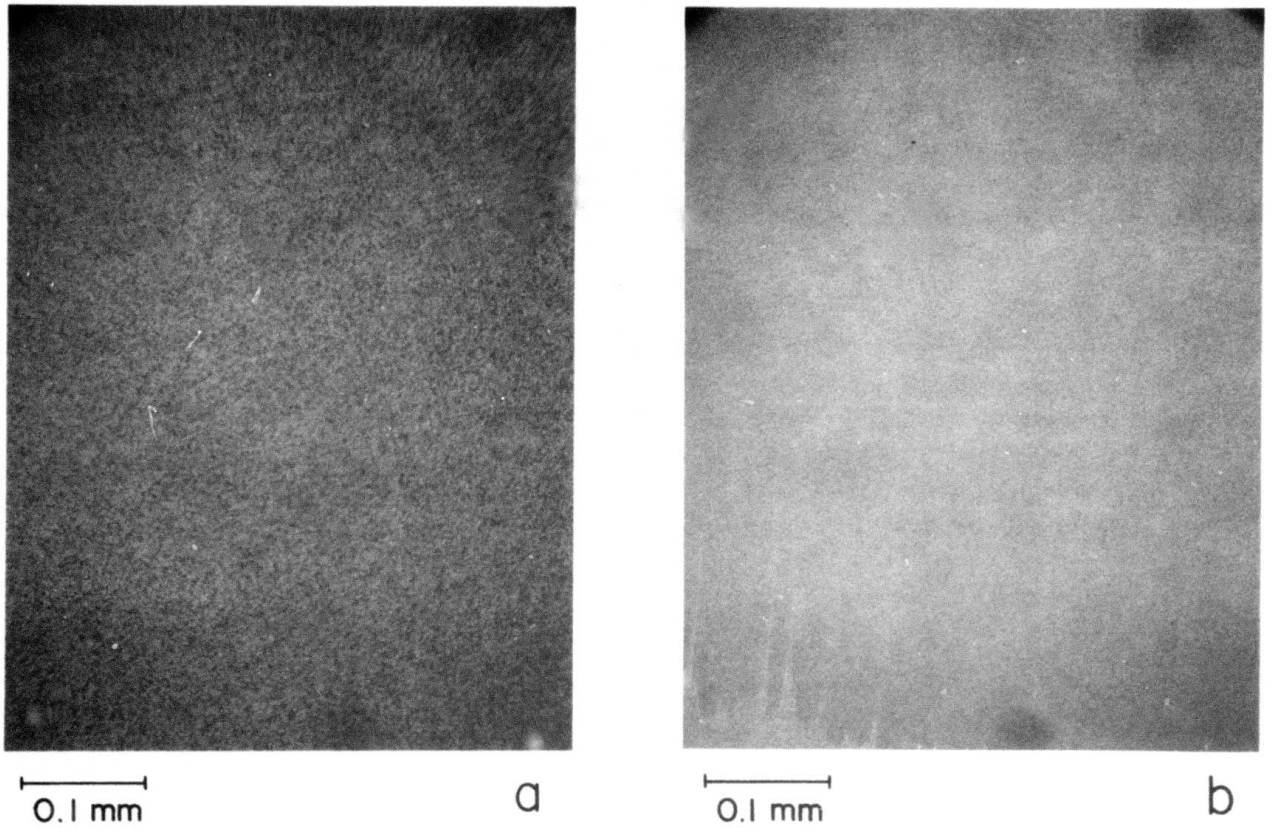



FIGURE 2-2. OPTICAL MICROPHOTOGRAPHS OF (a) NONREFLECTIVE POLY FILM AND (b) REFLECTIVE POLY FILM

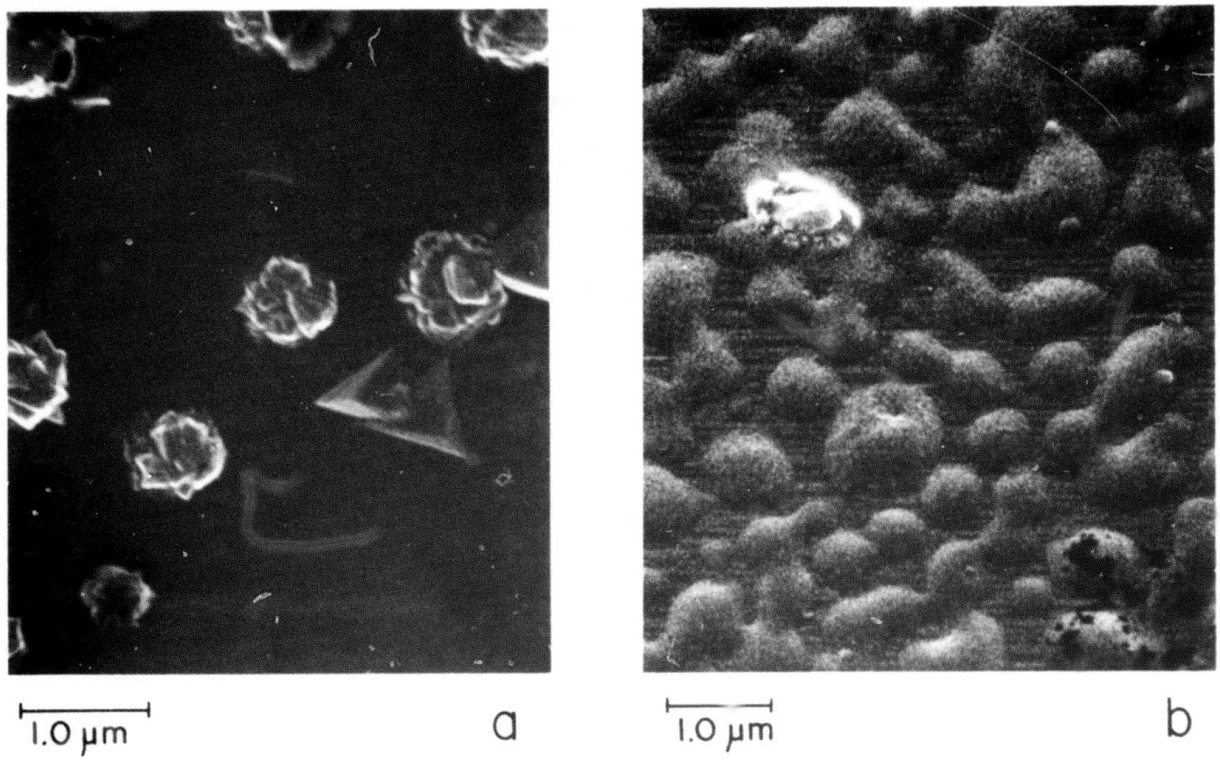



FIGURE 2-3. SEM IMAGES OF POLYCRYSTALLINE FILM
(a) SAMPLE 1503, UNCOATED
(b) SAMPLE 1502, COATED WITH 200A Au-Pd

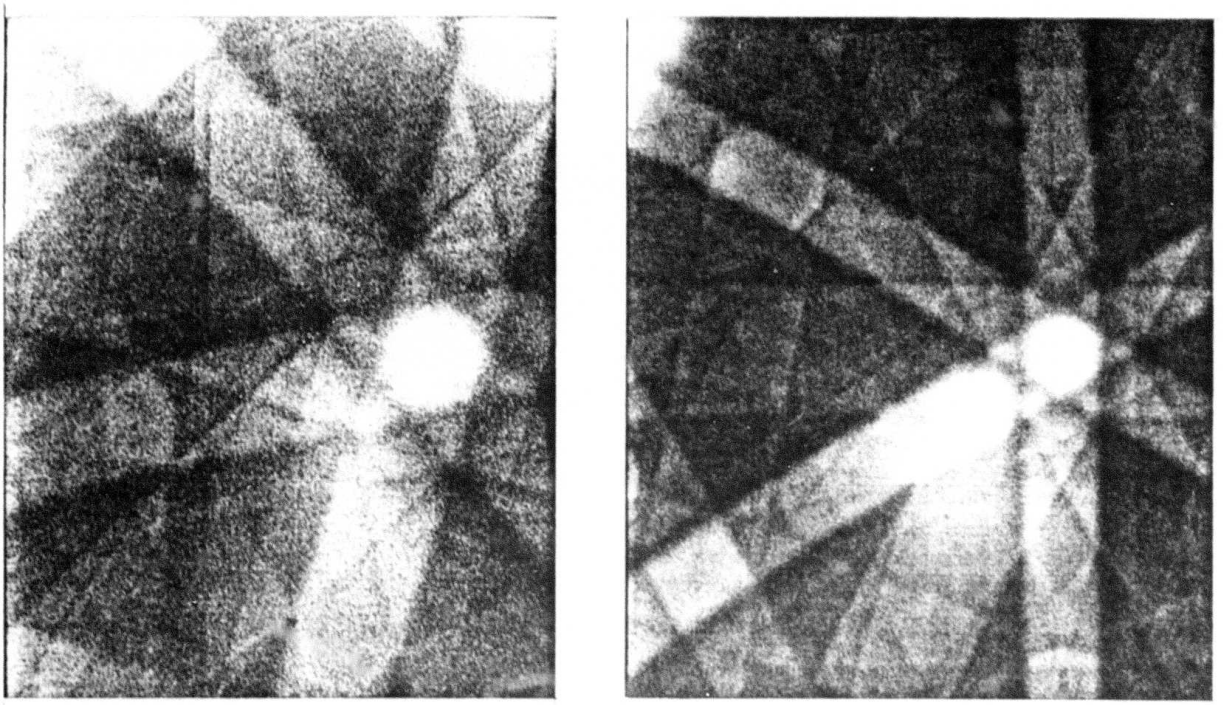



FIGURE 2-4. ELECTRON CHANNELING PATTERNS FROM NOMINALLY 0.5 MICRON THICK CVD FILMS

(a) POLYCRYSTALLINE

(b) EPITAXIAL

(Note: The difference between these patterns is a function of electron energy in microscope and film exposure. It does not represent a difference in the samples.)

Typical RHEED results are shown in Figure 2-5(a), (b), and (c) for low temperature CVD polycrystalline deposits. Figure 2-5(a) shows a strong ring structure, implying small grain randomly oriented polycrystalline material. This is typical of the expected results for this kind of deposition. Figure 2-5(b) shows weak ring structure and a strong dot pattern with weaker "echoes". The smaller dots, near and repeating the larger, stronger pattern, imply twinning of nearly single crystal material. This deposit is very strongly oriented in the (100) direction, and rotation about one axis of the different crystallites has produced the twinning effect. The deposit shown in Figure 2-5(c) is characterized by the strong Kikuchi lines characteristic of high quality single crystal material, plus weak dot and ring patterns. Kikuchi patterns are collective effects of diffraction from large crystals with long range order. Their presence implies epitaxial crystal growth, with some random ordering deduced from the weaker patterns.

The doping profile of the deposited polycrystalline layer was measured by SIMS.[9]. This technique cannot detect impurity concentrations below 0.01 atomic percent (about $5 \times 10^{18}/cm^3$ in silicon) and is accurate only above 0.1 percent. Figure 2-6 shows that arsenic dopant from the substrate, about $3 \times 10^{19}/cm^3$, was deposited in the polysilicon film during deposition. The dopant concentration falls off from the value at the film-substrate interface, but does not go to zero. The residual concentration of arsenic does not exceed $5 \times 10^{18}/cm^3$. Zero level detection of arsenic in silicon can be seen in Figure 4-8, implying that the detected presence is real, although it is near the detection limit of this analytical technique.

The source of the dopant is not clear. Near the film-substrate interface the dopant profile follows the predicted diffusion profile[10] for the autodoping of epitaxial CVD films. The estimated diffusion coefficient, D, is $3 \times 10^{-15}$ $cm^2/sec$. This is derived from Figure 2-6 by estimating the distance for the concentration to drop by 90 percent to be $500A = 2(Dt)^{1/2}$. The deposition time is given in Table 2-1. The value of D corresponds to a temperature of about $950^{\circ}C$. Since this is higher than the measured (by pyrometer) temperature of the substrate, it implies either an excess of diffusion along grain boundaries or some additional doping mechanism. The steady level of arsenic concentration near the surface of the film is not predicted by diffusion theory. Since dopant was not added to the gas mixture during deposition, it must have come from the

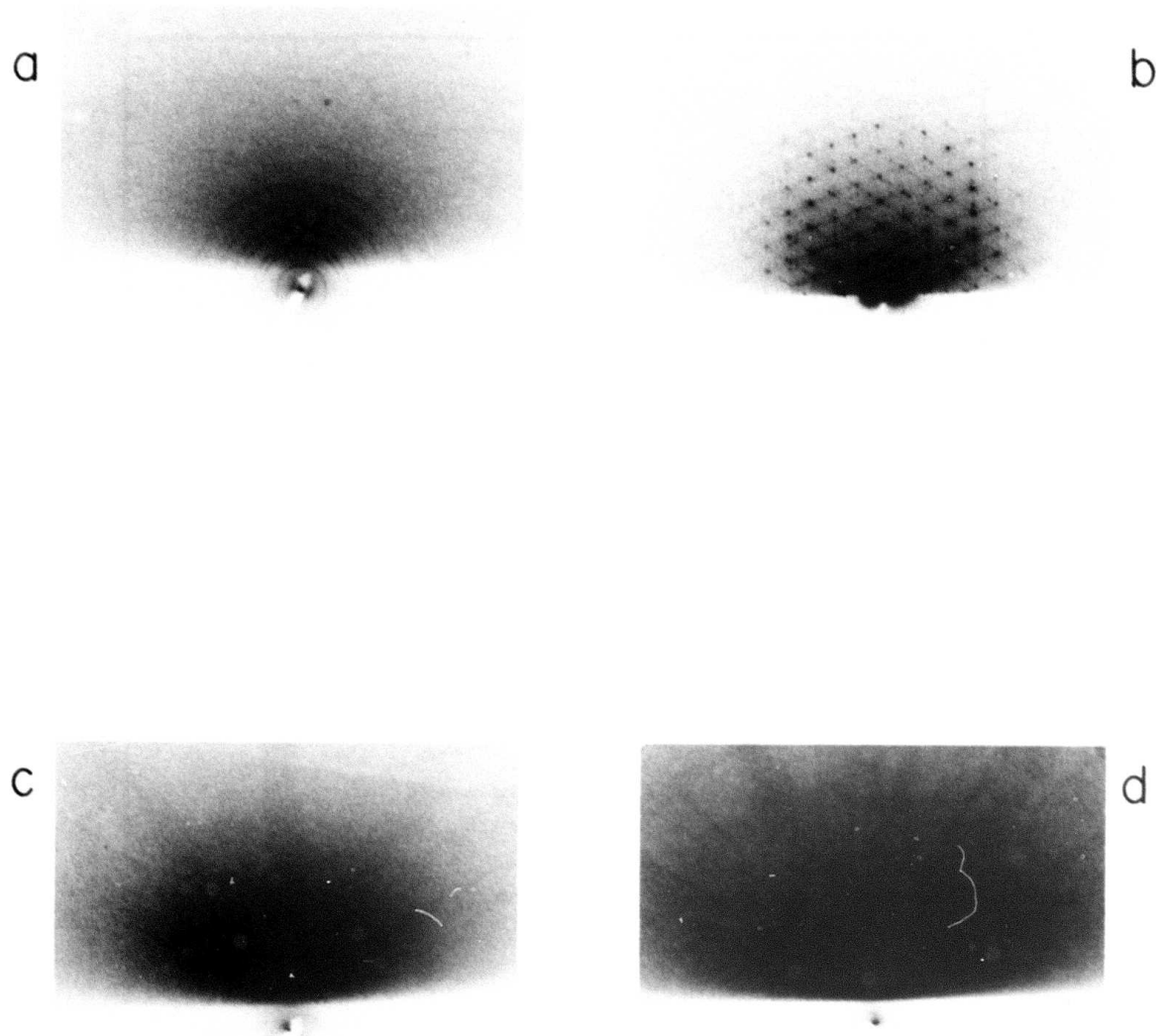



FIGURE 2-5. RHEED PATTERNS FROM POLY (a, b, c) WITH SUCCESSIVELY BETTER ORDER AND GOOD SINGLE CYRSTAL EPITAXIAL LAYER (d)

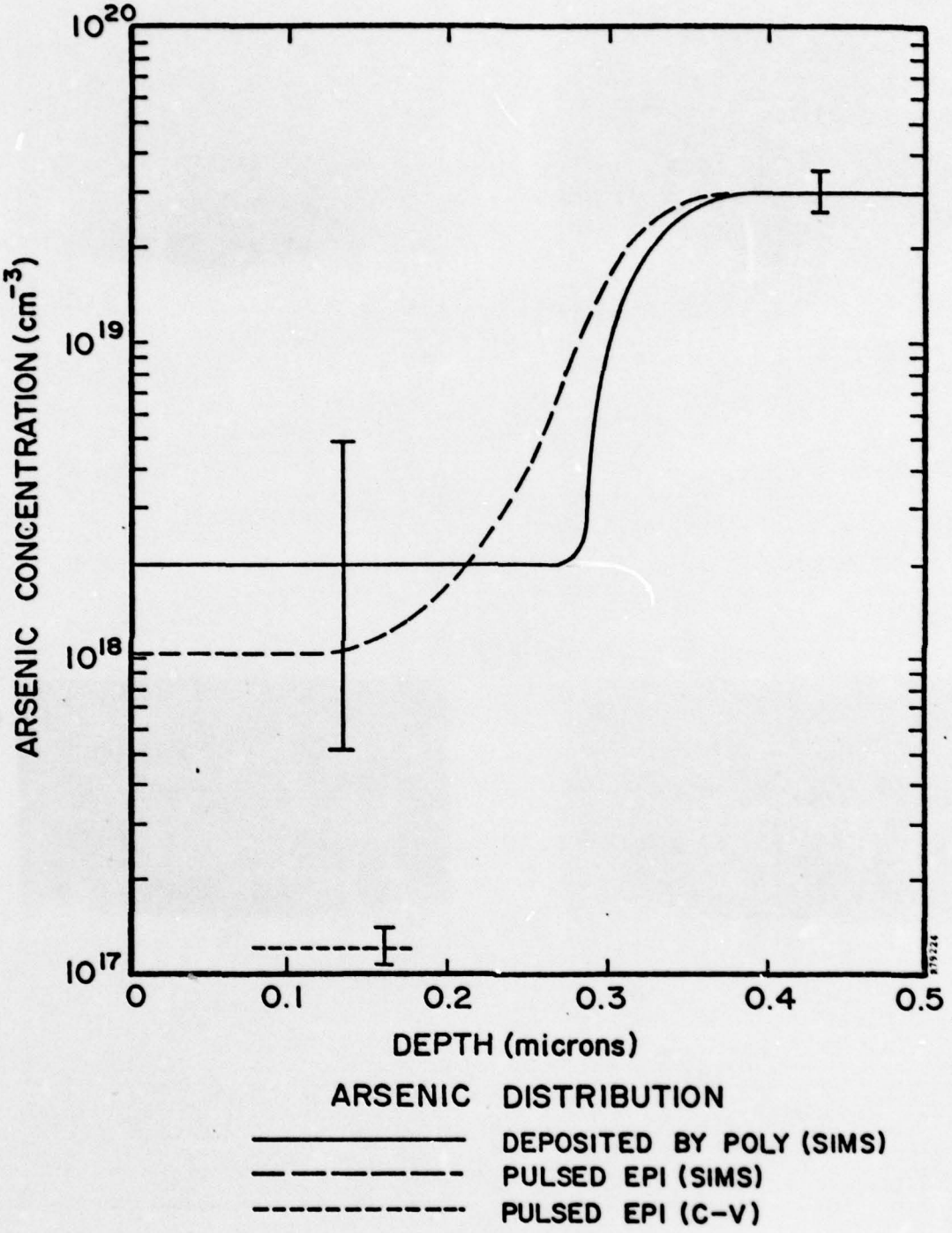



FIGURE 2-6. DOPANT PROFILES IN AS-DEPOSITED POLY FILMS AND AFTER PULSED ELECTRON BEAM EPITAXY

wafer. This is not likely to be out-diffusion from the wafer surface at 840°C. A high temperature step used for cleaning prior to deposition, 1000°C for 10 minutes in hydrogen alone, could have removed some arsenic from the substrates and deposited it as a contaminant in the CVD reactor where it could be redeposited. This step was not revealed to the experimenter until after analysis, and it should not have been performed. Also, it appears that the production of high resistivity films (low dopant concentration) is different from depositing undoped films. These processing problems are a function of the type of reactor used, and a change is recommended.

## 2.4 HIGH TEMPERATURE CVD EPITAXIAL FILMS

The same reactor and gas mixture, silane in hydrogen, was used to deposit epitaxial silicon films on (111) arsenic doped substrates with a bulk resistivity of 0.003 ohm-cm. The wafer backs were sealed to reduce autodoping. Thin surface oxides were etched in HCl prior to deposition at 1050°C. Approximately 0.5 micron of silicon was deposited per minute. After removal from the reactor the films were smooth and unblemished and contained no surface features visible by microscopy.

The deposition was made with one slide having a quartz chip on it for absolute thickness measurement. However, as with the poly films the chip affected the deposit of silicon near it, so that the "step" was not sharp. Difficulty in maintaining level surface prevented accurate measurements with a DEKTAK, although results are given in Table 2-1. Because the dopant profile has no sharp step, other film measurement techniques will have some error. An infrared spectrophotometer was used to measure the width of the thickest film by reflection techniques, 2.45 microns compared to a nominal estimate of 3.0 microns. Results of a groove and stain test are shown in Table 2-1; all values are about 0.2 micron lower than the nominal thickness. All epi films were thinner than requested but within specifications for this type of process.

The doping profile of a CVD epitaxial film is shown in Figure 2-7. It was measured by SIMS and capacitance-voltage (C-V) analysis[11]. The C-V measurements could not be extended in depth because the depleted layer broke down near the very highly doped substrate. The C-V measurements are a more accurate determination of the film-substrate interface than SIMS. The interface is defined as the point where the concentration falls by 50 percent[10], or about 0.4 micron in Figure 2-7. From the computations in Reference (10), and the drop of dopant concentration by a factor of 10

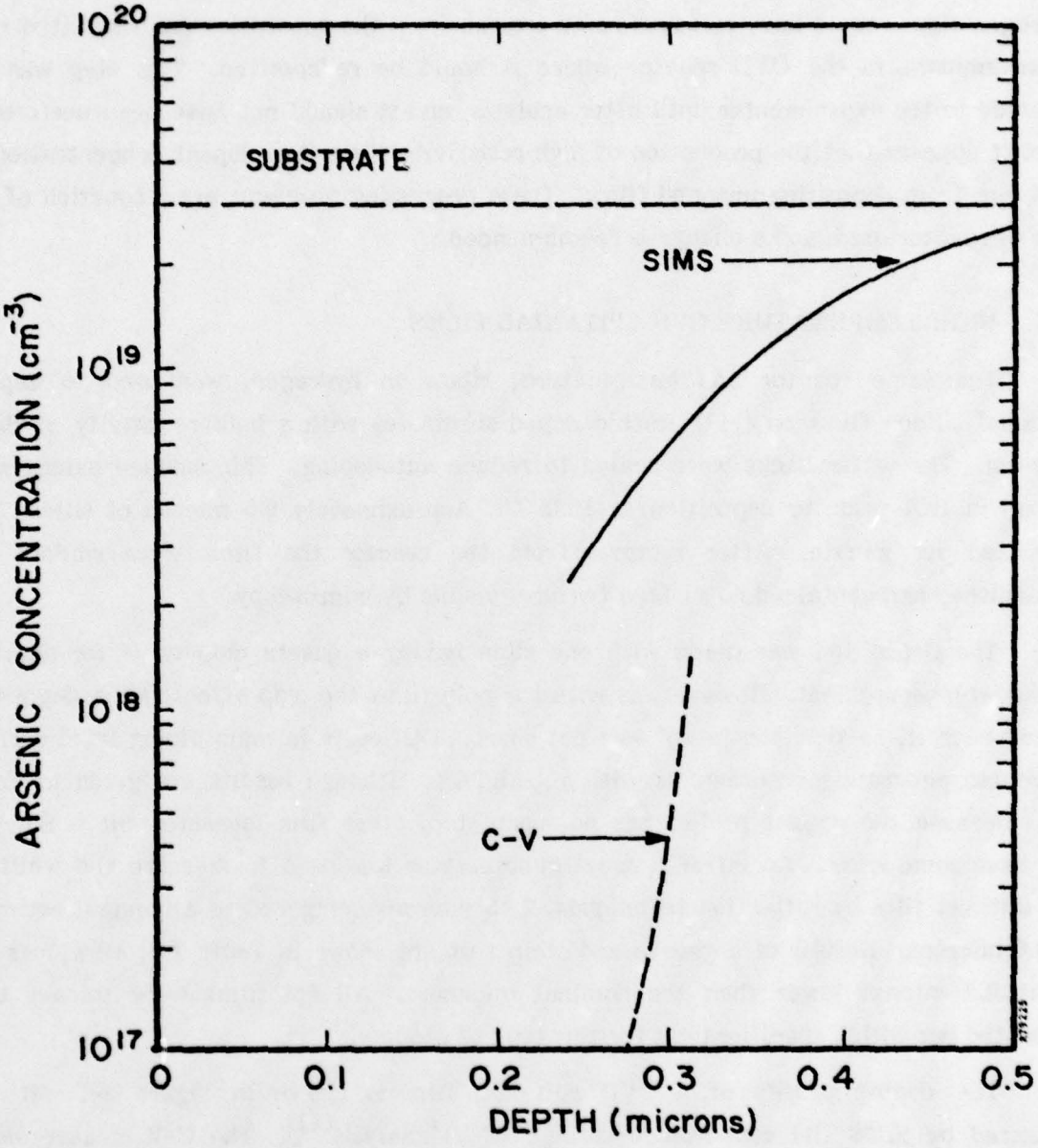



FIGURE 2-7. DOPANT PROFILE IN CVD EPITAXIAL SILICON

(SIMS data) at a depth of 0.25 micron, the diffusion coefficient would be approximately $1.5 \times 10^{-12}$, implying a temperature of 1300°C. From the C-V data the interface region is narrower and the temperature implied by the data lower. This would correspond to the actual temperature during deposition of 1050°C.

The crystalline aspects of the epitaxial films were analyzed by electron channeling (see Figure 2-4a) and RHEED (see Figure 2-5d). The channeling analysis is identical to that of a strongly aligned poly film. The RHEED pattern shows only Kikuchi lines—no spots and no rings—indicating very well ordered material.

## 2.5 FUTURE DEPOSITION PLANS

From the analysis performed, the polycrystalline layers deposited to date show two undesirable characteristics:

- The films are highly doped.
- The crystal grains are well aligned to the substrate.

The doping level is unsuited for the devices we would want to demonstrate, and the crystal structure makes it difficult to define accurately the effect of pulsed epitaxy. To correct both problems, deposition temperatures must be lowered, which is possible but not feasible in the epitaxial film reactors at Spire. In the next quarter, three different deposition techniques will be tested:

1. Low temperature, infrared heated CVD reactors
2. Low pressure CVD
3. Plasma ion deposition

Samples are now in process for LPCVD films. Additionally, epitaxial films will be deposited on lower doped substrates, with and without a buried layer, for future comparisons.

# SECTION 3
# PULSED EPITAXIAL REGROWTH

## 3.1 GOAL OF TASK 2

Deposition of epitaxial silicon films on single crystal substrates is easily achieved at high substrate temperatures but cannot be achieved at low temperatures, such as are desirable in this program. This task is to demonstrate that a chemically pure but poor crystallographic silicon films can be melted and regrown epitaxially without disturbing the dopant pattern in the underlying substrate. The final product must be suitable for making devices.

The objectives for this task are to (1) analyze the pulsed epitaxy requirement for VLSI technology, (2) develop and characterize a pulse electron beam(s) to meet these requirements, (3) demonstrate pulsed epitaxial regrowth of silicon films, and (4) compare these films to conventional CVD epitaxial structures.

## 3.2 ANALYSIS OF PULSED EPITAXY REQUIREMENTS

Requirements for epitaxial silicon layers vary with different technologies. As device size shrinks, the epitaxial layer thickness will also be reduced. It now appears that most requirements for VLSI can be met with layers 0.2 to 1.5 microns thick and, possibly, as thick as 3.0 microns. Uniformity requirements are approximately $\pm 10$ percent for film resistivity. This is a summary of $I^2L$, MOS, and conventional bipolar technology. Additional data is presented in Table 3-1.

The epitaxial layer thickness and doping in an $I^2L$ device are extremely important design parmeters and must be precisely controlled. Future requirements[12] start at 1.2 microns and scale downwards to 0.2 micron as surface geometries shrink from 1.5 to 0.5 micron line widths.

The epitaxial layer thickness is a relatively unimportant part of an MOS device. The principal minimum limit on this parameter is the thickness required to maintain the breakdown voltage of the transistor drain. The maximum limit is determined by the surface area allotted to diffusion isolation of devices, which must increase when the epitaxial layer becomes thicker. For VLSI applications, short channel lengths and shallow junction depths will be used[13], reducing the operating voltages. As a result, epitaxial layer requirements will be between 1.0 and 3.0 microns, with doping controlled to roughly a factor of two.

TABLE 3-1. EPITAXIAL LAYER THICKNESS ANTICIPATED FOR VLSI

| Technology | Minimum Line Width | Optimized Epitaxial Layer Thickness (microns) | Dopant Uniformity or Sheet Resistance (microns) |
|---|---|---|---|
| $I^2L$ | 1.5 | ±10% | 1.2 |
| | 0.5 | | 0.2 |
| MOS | 1.0 | ±30% to 50% | 1.0, 1-3 range |
| Convention Bipolar | 1.0 | | 1.0, 1-3 range |

In conventional bipolar technologies, the epitaxial layer serves as the collector of the individual transistor. The minimum epitaxial layer width is that necessary to support the specified breakdown voltage. With lower voltages and heavily doped collectors this limit is less than 1.0 micron. The maximum width is determined by device speed (which is faster for thinner collectors) and by the area consumed in isolation tubs. For bipolar technology a typical design goal for the epitaxial layer width is between 1.0 and 3.0 microns.[9]

## 3.3 ANALYSIS OF AUTODOPING DURING PULSED EPITAXY

This section covers a computer model of dopant diffusion during pulsed epitaxial regrowth of a deposited layer. There will be negligible diffusion of impurities or added dopants in material which remains solid during the pulsed heating process. This calculation instead estimates the amount of diffusion expected from the buried layer in the liquid phase and shows the control required to minimize this contribution to autodoping. The substrate, and buried layer, are not melted intentionally. But the silicon film overlying the buried layer must be melted completely for good epitaxy, and the allowable variation in depth of melt (which must then extend into the substrate) must be determined.

The typical time required for heating the film to the melt point is 0.1 microsecond, much less than the time required to cool the layer by thermal diffusion. The cooling time required for freezing the melt is approximately 1.0 microsecond. For common dopants near the melt temperature, the diffusion coefficient is approximately $10^{-11}$ $cm^2/sec$[15]. The approximate diffusion length scale in one microsecond $(Dt)^{1/2}$ is therefore less than 1A, and justifies the assumption of negligible diffusion in the solid phase.

Diffusion in liquid silicon is approximately $3x10^{-4}$ $cm^2/sec$[16]. In pulsed epitaxy the liquid is cooled from the bottom by conduction and freezes first from the deepest part. The time the silicon remains a liquid is greatest at the surface, is least at the maximum depth, and varies roughly linearly for thin films. In the calculation performed here the freezing interface was assumed to move at a constant velocity of 0.5 m/sec[17]. Diffusion of an unspecified dopant is at a constant rate (assumed) in the liquid and zero at any depth after freezing. Varying the diffusion coefficient with time prevents solving the diffusion equation analytically but allows for a simple, finite-element numerical calculation to be performed on a computer.

For this calculation, the silicon film is assumed to be 0.9X thick, and the melt depth is taken as X. In Figure 3-1 the value of X is 1.0 and 3.0 microns, respectively. The initial dopant concentration is taken as $10^{19}/cm^3$. The calculation shows that the dopant concentration in the film after cooling falls by three orders of magnitude in 1.0 micron, between the maximum melt depth and the surface. For the 3.0 micron melt depth, the total amount of dopant in the film is greater because the depth of melt into the substrate is greater.

This is a worst case calculation. It assumes that the dopant source in the substrate is infinite, whereas the dopant source is only a shallow diffused or ion-implanted region near the surface of the substrate. The calculation also assumes that the depth of melt into the substrate or buried layer is about 10 percent of the thickness of the film. This figure can be reduced by better control of electron beam uniformity and average fluence.

The melt depth will vary approximately linearly with the beam fluence. This is shown in Figure 3-2, a computer model of melt depth versus fluence for crystalline (X-Si) or amorphous ( -Si) silicon samples. The pulsed electron beam is assumed to have a constant energy spectrum[18]. The fluence required to melt a small-grain polycrystalline sample lies between these two curves. The effect of 1 micron of -Si over a crystalline substrate is also shown. Note that the melt depth is very sensitive to the fluence below 0.5 micron, but varies almost linearly with electron beam fluence for thicker films (over 1 micron). Also, the calculation for a 1 micron film shows a large change in slope near the interface. This implies that control of melt depth for the films of interest is practical. This study will be extended using different electron beam energy spectra to determine whether improved control of melt depth, and therefore doping, is possible.

## 3.4 PULSED ELECTRON BEAM DEVELOPMENT

For pulsed electron beam epitaxy a change in the beam used for annealing was deemed necessary. The previously used electron beam[18] has an angle of incidence of about 60 degrees (average) and has been optimized for peak surface dose on silicon. It is typically used to melt between 0.2 to 0.3 micron of amorphous silicon and shows a strong tendency to cause thermal stress damage to substrates as the fluence is raised. To melt thicker films a more normally incident beam is considered desirable. Maintaining the same diode characteristics and electron energy spectrum, the sample mounting was

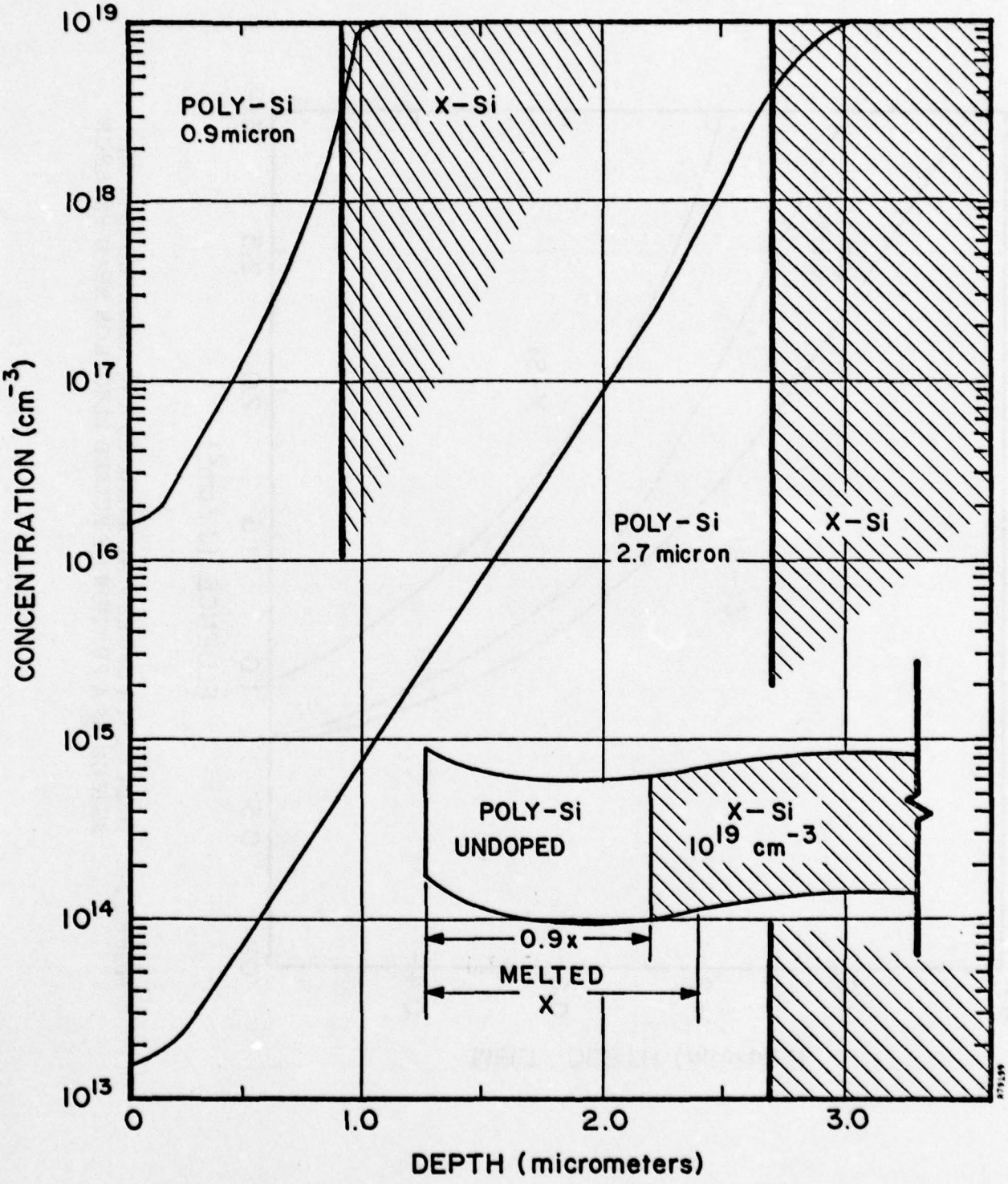



FIGURE 3-1. DIFFUSION OF DOPANTS FROM SUBSTRATE INTO PULSED ELECTRON BEAM EPITAXIAL FILMS

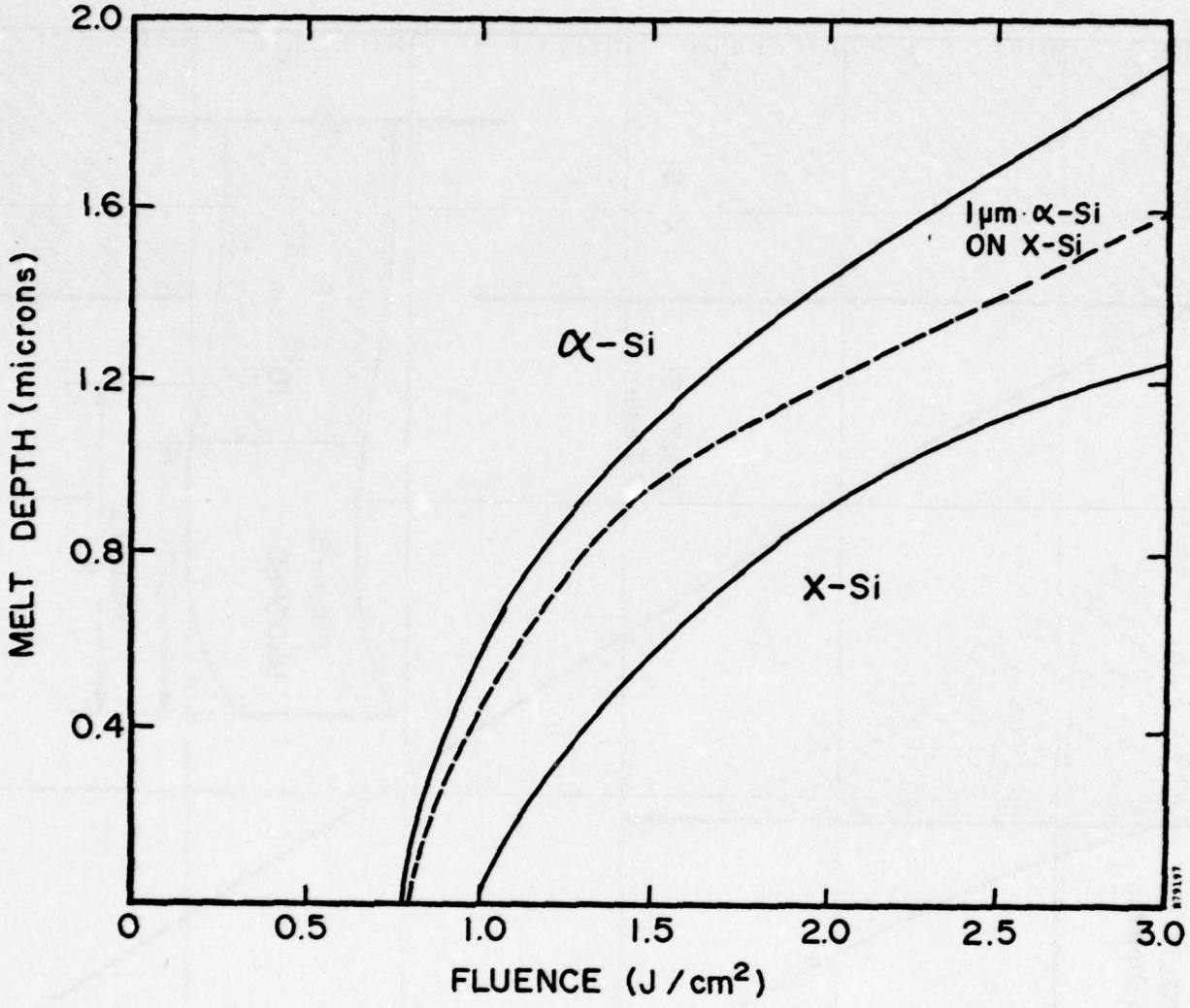



FIGURE 3-2. MELT DEPTH IN CRYSTALLINE (x-Si) AND AMORPHOUS (α-Si) SILICON AS A FUNTION OF PULSED ELECTRON BEAM FLUENCE

modified to change the self-focusing characteristics of the beam. Figure 3-3 shows the calibration of fluence versus charging voltage for the new and old beams, Figure 3-4 shows the electron beam deposition profiles for typical pulses, and Figure 3-5 shows the initial temperature calculations performed. Changing the angle of incidence has lowered the surface dose for a given fluence, but will reduce thermal stress by reducing the temperature gradient. Stress calculations will be available in the next quarter.

## 3.5 EXPERIMENTS

A tabulation of all pulsed epitaxial regrowth work appears in Table 3-2. Quickly summarizing the results:

- Excellent epitaxial regrowth was observed for 0.3 micron films.
- Single crystal regrowth with some twinning was observed for 0.45 micron films.
- Doping profiles follow theoretical predictions.

The feasibility of pulsed epitaxial regrowth of thin polycrystalline silicon films has been demonstrated. For device quality results the doping level in the deposited film must be reduced. Extensive physical characterization of these films was performed and will be discussed next. Electrical characterization was limited to C-V measurements but will be expanded in the next quarter.

Optical characteristics of the films after pulsing were changed, especially for initially nonreflective samples. A circular spot, corresponding to the beam diameter, was changed from a dull gray to a mirror finish. Before and after pictures would very much resemble the reflective and nonreflective films in Figures 2-2(a) and (b). Under an optical microscope there was no visible change in initially reflective, smooth films. At high power, about 50 percent greater fluence than the required threshold values, cracks and/or pitting of the surface became visible. Cracking is considered a thermal stress phenomena and can be avoided by appropriately tailoring beam parameters to film thickness and stoichiometry. Pitting or cratering is attributed to excess beam flux in the diode which can partially melt the refractory anode mesh. Small droplets of this material damage the sample. This is also avoided by the appropriate choice of parameters. No visible damage occurred at the correct choice of fluence for these thin films.

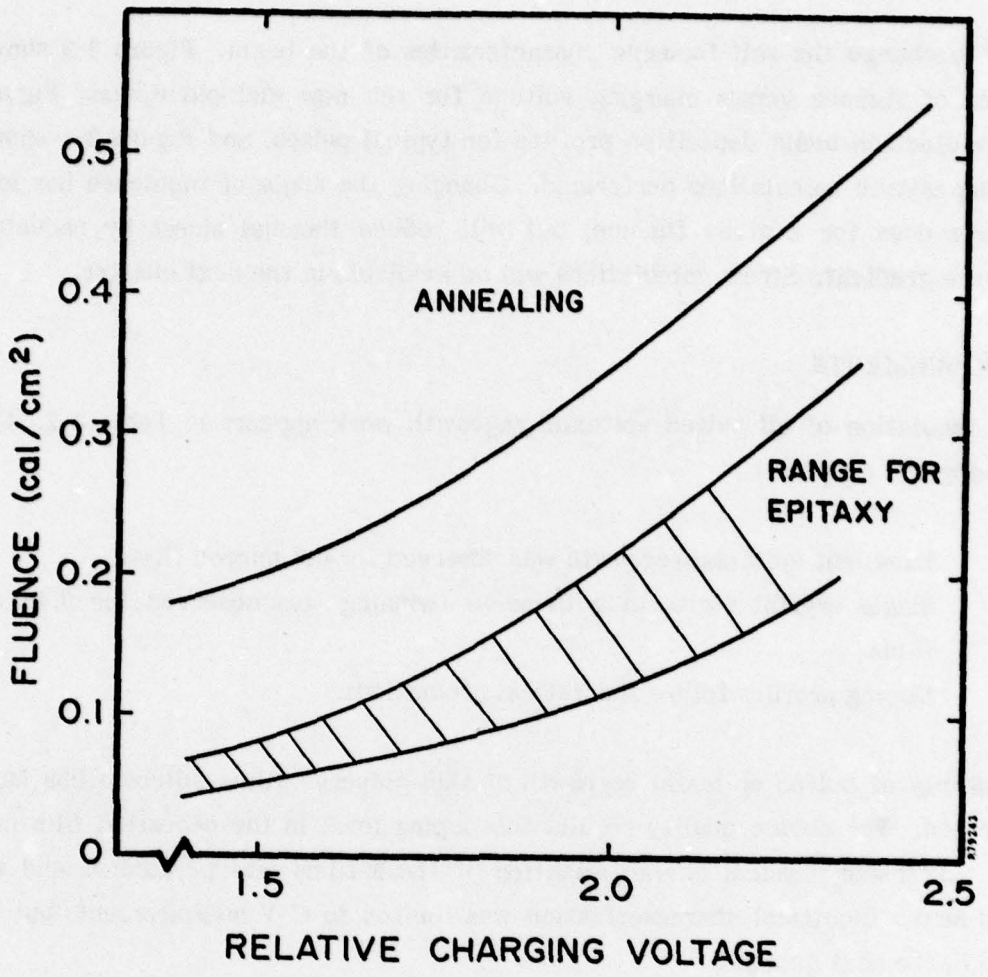



FIGURE 3-3. PULSED ELECTRON BEAM FLUENCE FOR ANNEALING AND FOR EPITAXY (Note: At constant charging voltage, electron energy spectrum is identical. Beam for epitaxy can be focused onto target within range shown.)

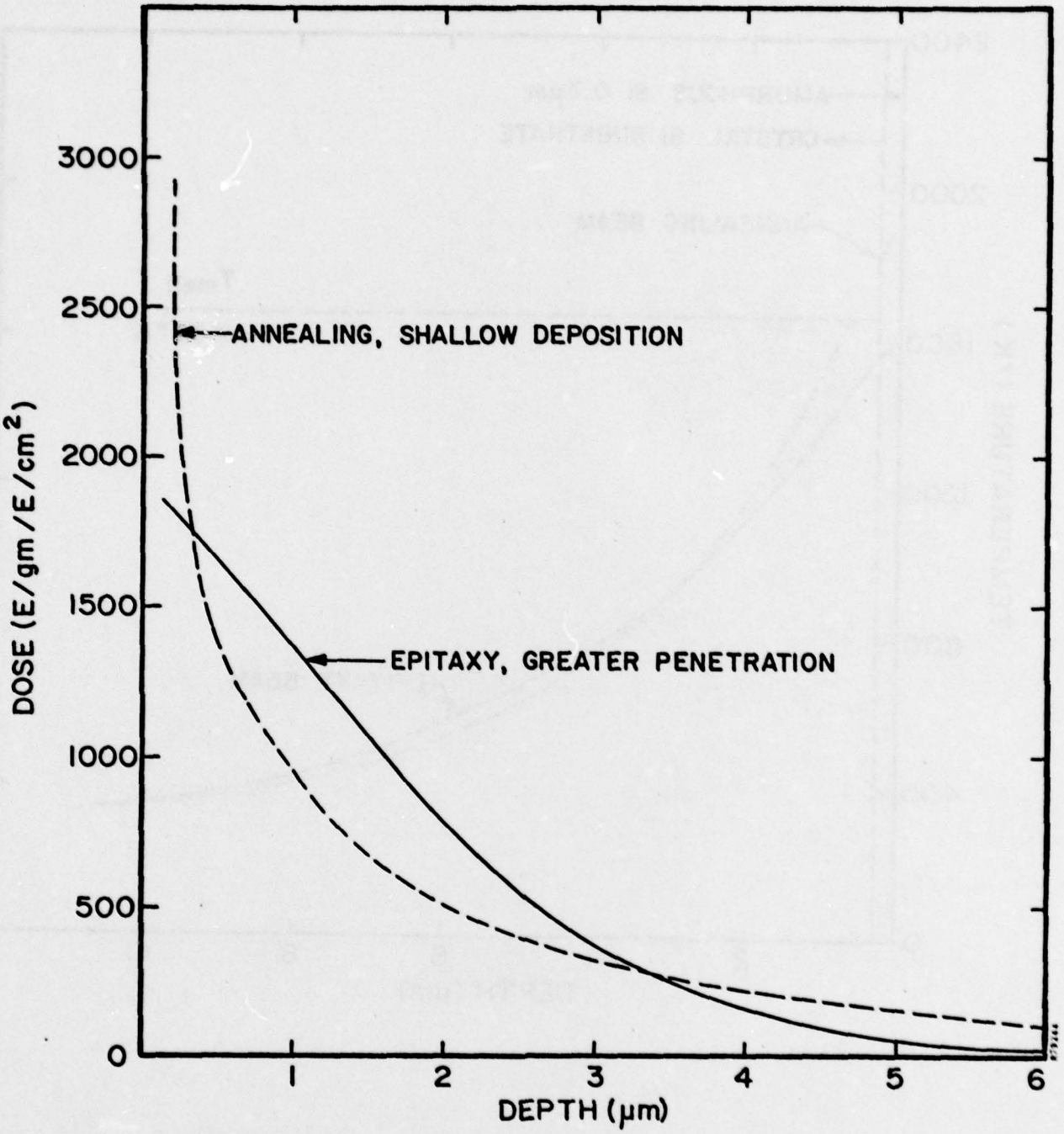



FIGURE 3-4. DEPTH DOSE PROFILE

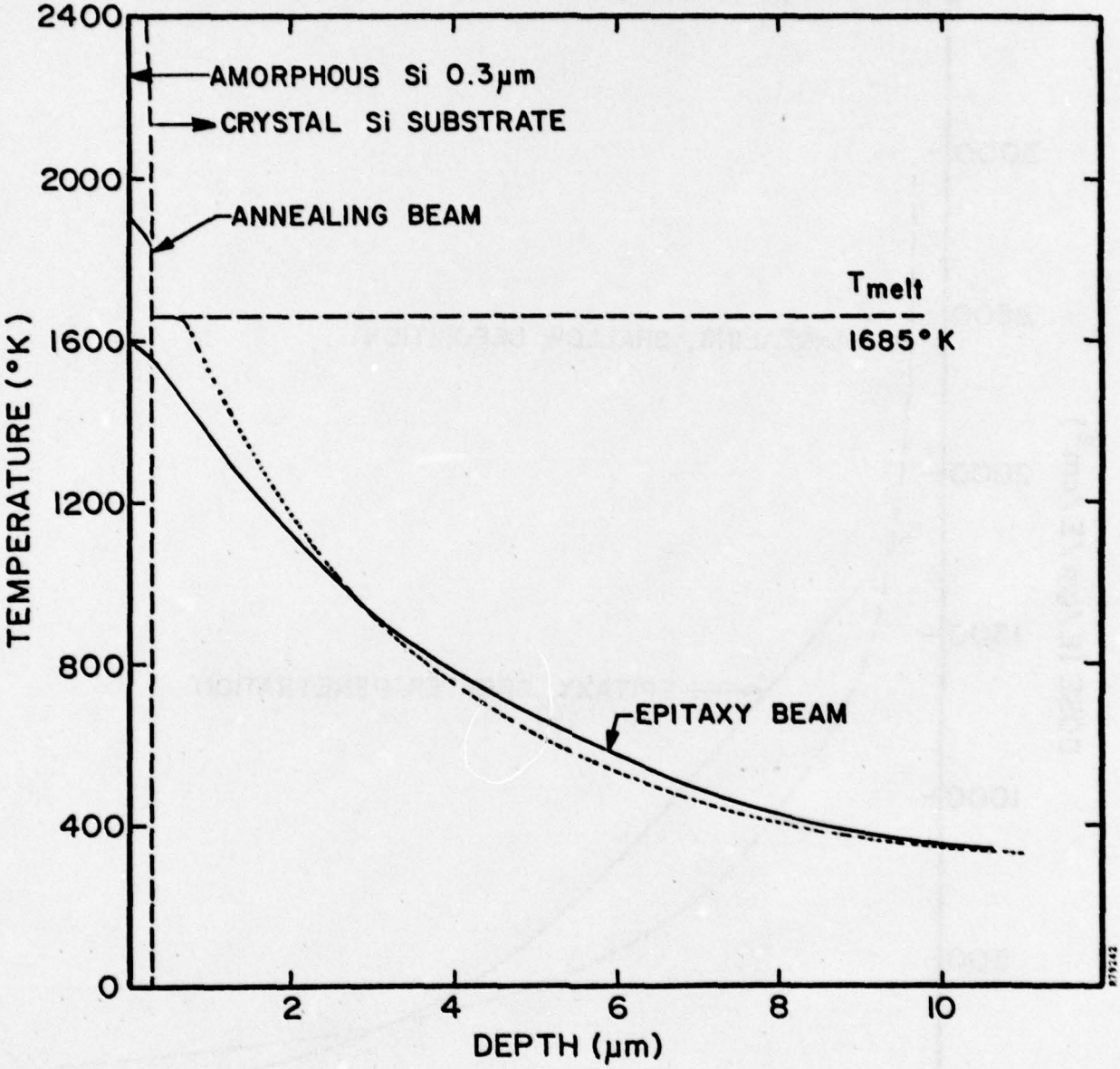



FIGURE 3-5. TEMPERATURE VERSUS DEPTH PROFILE
(Note: At time of maximum surface temperature; fluence = 0.24 cal/cm$^2$)

TABLE 3-2. LISTING OF ALL PULSED EPITAXIAL EXPERIMENTS

| Film ID No. | Pulse ID No. | Fluence ($cal/cm^2$) | Comments |
|---|---|---|---|
| 1499 | — | 0.16 | no visible change |
| | — | 0.20 | cracked |
| 1502 | 20043 | 0.20 | no visible change |
| | 20044 | 0.26 | visible pattern |
| | 20045 | 0.29 | visible pattern |
| | 20046 | 0.34 | cracked in center of pattern |
| 1503 | 19051* | 0.20 | SEM, SIMS, C-V, RHEED analysis |
| | 19058 | 0.17 | faint pattern |
| | 20050 | 0.20 | faint pattern |
| | 20051 | 0.26 | broke, largest piece lost |
| | 20052 | 0.29 | 1.5 cm o.d. pattern, cracks in center |
| | 20053 | 0.34 | broke from pulse, 2.0 cm spot, cracks |
| 1974 | 19562 | 0.18 | no change |
| | 19574* | 0.22 | good, C-V implies 1 ohm-cm film, given COTR |
| | 20057 | 0.20 | small pattern |
| | 20058* | 0.25 | possible junction in substrate |
| | 20059 | 0.29 | broke, pattern "wavy", melted |
| | 20060 | 0.34 | broke, pattern "wavy", pitted |
| 1971 | 20064 | 0.2 | no visible pattern |
| | 20065 | 0.25 | no visible pattern |
| | 20066 | 0.29 | no visible pattern |
| | 20067 | 0.34 | arc near corner, wavy, cracks, pits |
| 2035 | 20072 | 0.29 | no visible pattern |
| | 20073 | 0.34 | no visible pattern |

*C-V analysis possible, no short at low voltage bias.

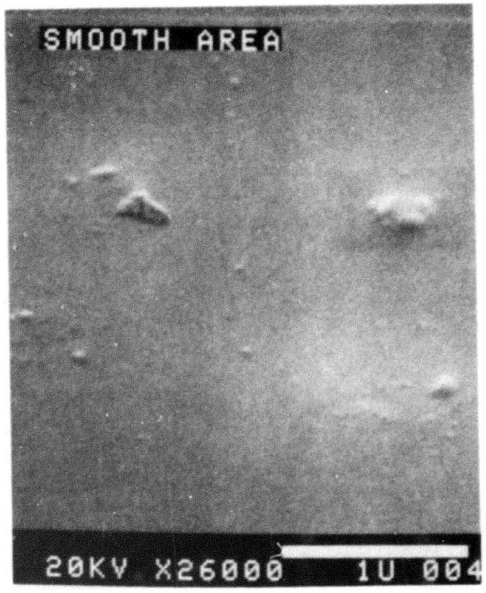
Before and after pulsing SEM photos are shown in Figure 3-6[8]. The sample is from lot 1503, and the same sample was used for electron channeling, reflected diffraction, SIMS and C-V analysis. Before pulsing, the surface of the sample is characterized by 0.5 micron raised structures and polycrystalline grain boundaries on the flat surface. After pulsing, the raised structures have been melted and substantially reduced to a nearly flat plane and the grain boundaries are no longer visible.

A combined transmission electron microscope/scanning electron microscope (TEM/SEM) electron microscope with electron channeling, transmission and reflected diffraction capability[7] was used to characterize the crystalline structure of the material. Channeling measurements were not useful (see Figure 2-4) because they could not distinguish between the deposited poly and epitaxial material. RHEED patterns are shown in Figure 3-7(a) before and (b) after pulsing. Figure 3-7(a) is a duplicate of Figure 2-5(b). Comparing Figure 3-7(b) to Figure 2-5(c) and (d), the recrystallized material shows no evidence of polycrystalline rings and has very strong Kikuchi lines similar to the epitaxial film. This is strong evidence for excellent epitaxial regrowth. RHEED patterns of thicker poly films, before and after pulsing, are shown in Figure 3-8. A significant change in structure is visible. However, the final pattern is characteristic of twinned crystal, rather than the quality material seen in Figure 3-7. No evidence for polycrystalline structure is visible in Figure 3-8(b).

The doping profiles of the pulsed films in sample 1503 were measured by SIMS and C-V analysis (Figure 2-6). The SIMS profile is compared to a calculated profile in Figure 3-9 which allows for melting 300A into the substrate below the film. They are reasonably similar. The steady doping level near the middle of the film shown by C-V analysis is suspected of being in the initially deposited poly (Figure 2-6) All pulsed films were measured by C-V analysis using a mercury probe for contacts. However, most of the samples had a very low breakdown voltage and could not be measured. Those samples which could be measured showed nearly identical results to Figure 2-6.

BEFORE

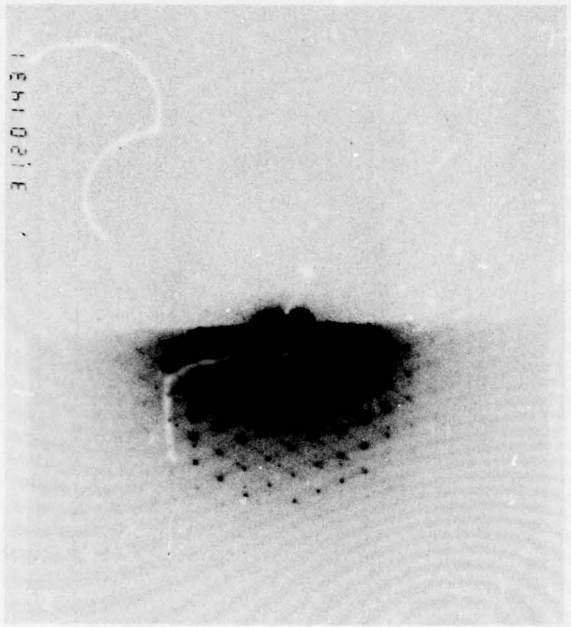
AFTER

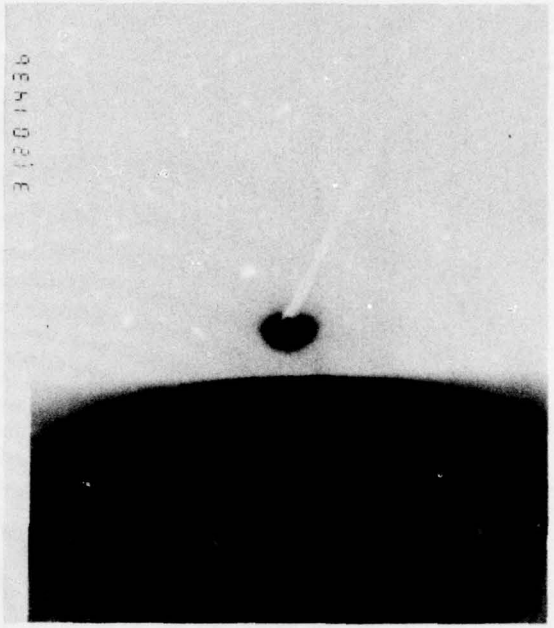




SEMS (x25,000) OF 3000 Å, 800°C CVD POLY-Si
BEFORE AND AFTER PULSE ELECTRON BEAM RECRYSTALLIZATION

BEFORE

AFTER





RHEED PATTERNS OF 3000 Å, 800°C CVD POLY-Si
BEFORE AND AFTER PULSE ELECTRON BEAM RECRYSTALLIZATION

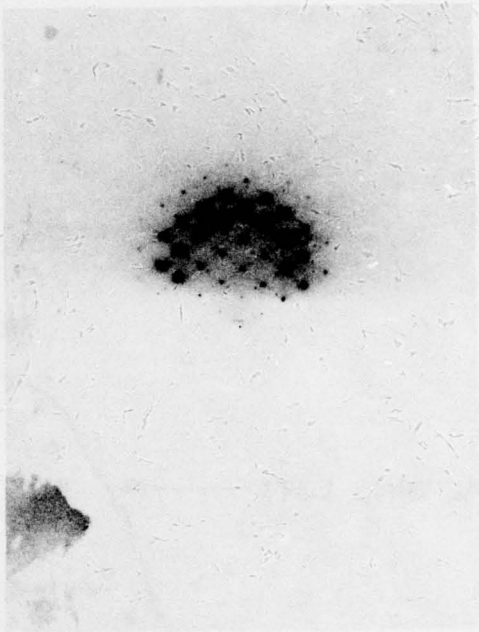


FIGURE 3-8. RHEED PATTERN OF INCOMPLETE PULSED EPITAXY EXPERIMENT SHOWING REGROWTH OF SINGLE, TWINNED CRYSTAL SURFACE (Note very weak poly ring pattern. Sample 1974 shot 20060.)

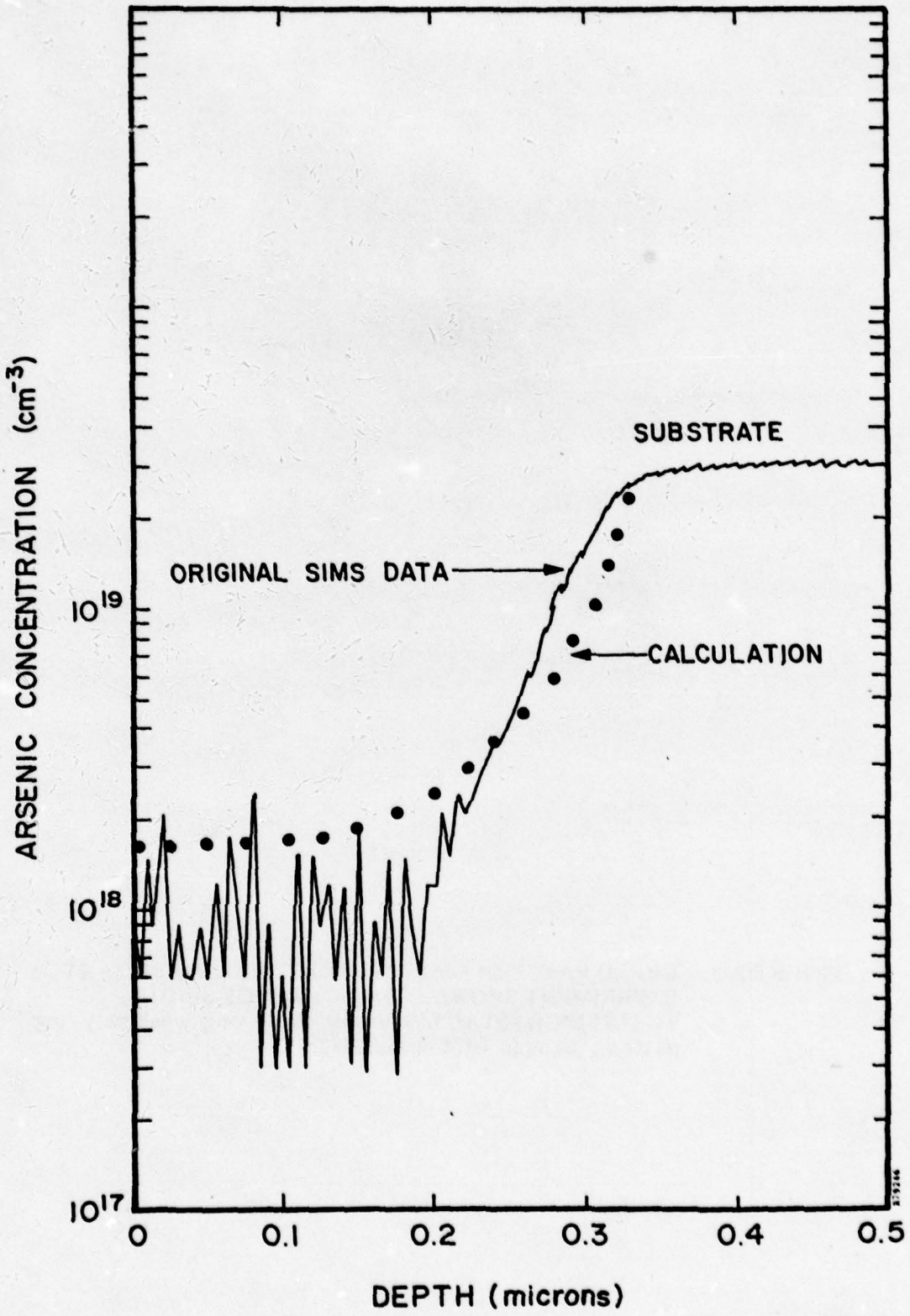



FIGURE 3-9. MEASURED AND CALCULATED ARSENIC DOPING PROFILES IN PULSED ELECTRON BEAM EPITAXY

## 3.6 CONCLUSIONS AND FUTURE PLANS

Epitaxial regrowth was demonstrated for thin films but not over 0.5 micron thick. Since the fluence was varied over a wide range, electron beam parameters such as energy spectrum and fluence would have to be changed in future tests with thicker films. The experiment to test the effect of oxide or no oxide etch prior to depositing the film failed due to the high crystal quality of the poly. This experiment will be repeated using films deposited at lower temperatures. Since the deposition technique was insufficient to test doping levels at the surface of the pulsed films, it will be changed according to Table 1-1. Also, since C-V analysis and defect measurements are limited by the very highly doped substrate, lower doped substrates in the 1-10 ohm-cm range will be used. Diffused or ion-implanted buried layers will be used to check for autodoping in the future.

## SECTION 4
## LOW TEMPERATURE JUNCTION FORMATION

### 4.1 GOALS OF TASK 4

This task will study the use of ion-implantation and pulsed electron beam annealing to form junctions of varying depths in silicon. The key goal is to maintain low substrate temperatures and to avoid diffusion in underlying layers when annealing damage in the surface. There are two approaches — liquid and solid phase annealing mechanisms. Liquid phase anneal is similar to pulsed epitaxy in that the surface is melted to a specified depth. Regrowth of the crystal structure from the melt[18] is excellent. The implanted dopant is nearly completely substitutional although diffused in the melt phase. Solid phase annealing is very similar to annealing in a furnace but uses higher temperatures and a large thermal gradient to force better crystal regrowth in the damaged region. Crystal growth rates are slower in the melt, so that more than one pulse, on longer pulses, are required for solid phase annealing. That the technique can work is shown by scanning electron beam experiments[19]. Without melting, the dopant will not be diffused from the original implanted profile and very fine geometry multiple layer structures can be preserved.

### 4.2 DETERMINE ANNEALING REQUIREMENTS

No matter what type of circuit technology is used for VLSI applications, it is unlikely that implant parameters will exceed the range $10^{12}$ to $10^{16}$ ions/cm$^2$ for surface dose[12]. Depth of junctions will vary greatly but will tend to be shallow as given in Table 4-1. This table was constructed around the model bipolar integrated circuit shown in Figure 4-1. The model was proposed to obtain "ballpark" numbers for the types of implants and geometries we would have to consider for VLSI applications. It is typical of structures in linear or digital bipolar integrated circuits such as emitter coupled logic (ECL) types. The model is not a limit to the proposed studies.

The different types of implants shown in Figure 4-1 and Table 4-1 bracket the capabilities required. The buried layer is a high dose implant into the substrate. It must be annealed prior to pulse epitaxy and the crystal structure after annealing is very important. This is the layer of concern for dopant redistribution in pulsed epitaxy. High dose implants for isolation or for contacts to the buried layer must be diffused relatively deep — through the entire epitaxial layer. These implants can be annealed by liquid

TABLE 4-1. TYPICAL IMPLANTED LAYERS FOR ALL IMPLANTED BIPOLAR INTEGRATED CIRCUITS

| Layer | Typical or Proposed Implant | | | | Purpose and Notes |
|---|---|---|---|---|---|
| | Species | Dose (ions/cm$^2$) | Energy (keV) | $X_j$ Post-Anneal (microns) | |
| $N^+$ Buried | As | $6 \times 10^{15}$ | 50 | 1 | Lowers series resistance to collector. |
| $P^+$ Isolation | B | $6 \times 10^{15}$ | 200 | 2.5 | Isolates N type "tubs". Depth must be greater than epitaxial layer thickness. May require a channeling type implant. |
| $N^+$ Top | P | $3 \times 10^{15}$ | 200 | 2 | Lowers series resistance to collector. Not always required to be as deep as epitaxial layer. May require a channeling implant. |
| $P^+$ External Base | B | $3 \times 10^{14}$ | 30 | 0.5 | Provides handle to active base and heavily doped surface for ohmic base contact. |
| $P^-$ Active Base | B | $3 \times 10^{12}$ | 30 | 0.3 | For high speed transistors f $\gtrsim$ 2 GHz. |
| $N^+$ Emitter | As or P | $3 \times 10^{15}$ | 15 | 0.15 | |
| P Resistor | B | $10^{12} - 10^{15}$ | 30 | 0.3 | Forms resistors. In most cases the external base implant is used for this purpose and total resistance is determined by resistor geometry. However, some circuits may require a particularly light or heavy doping to make a special resistor of practical size. |

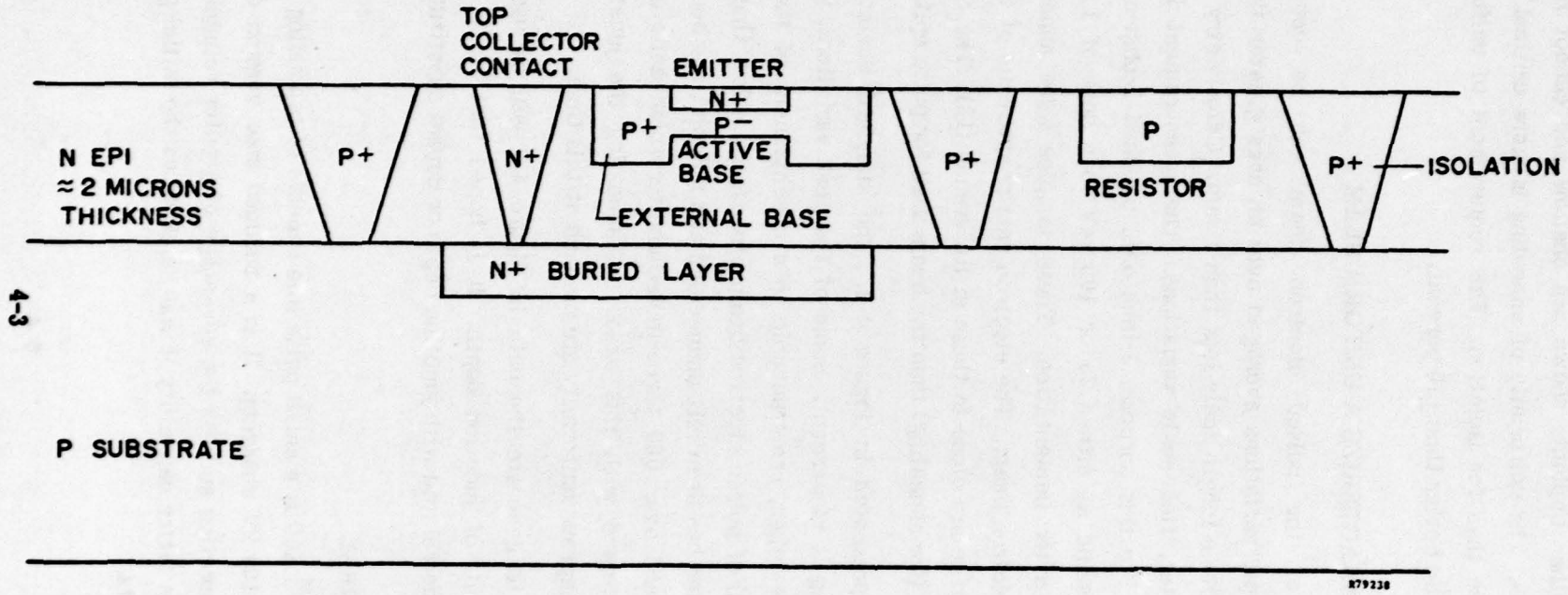





FIGURE 4-1. CROSS SECTION OF ALL IMPLANTED BIPOLAR INTEGRATED CIRCUIT

phase annealing. The Other implants shown are shallow and cannot be annealed with pulsed melting techniques. The uniformity of annealing is more critical for the implants forming the active device than for isolation. This requirement of uniformity is not yet specified but assumed to be better than ±10 percent.

## 4.3 DEVELOP AND CHARACTERIZE A UNIFORM BEAM

The uniformity of the pulsed electron beam can be considered on two levels — gross macroscopic variations averaged over an area greater than 1 $cm^2$ — and microscopic variations with a length scale less than 1 mm. Calorimetry can measure the former but not the latter, fine scale variations. The measurement is the processing uniformity on a wafer. For this purpose, 3-inch o.d., polished 1-ohm-cm silicon wafers were implanted with arsenic at either 25 or 100 keV to a dose of $1 \times 10^{16}/cm^2$. The surface was amorphous after implantation. These samples were annealed by a single pulse of a 3-inch o.d. electron beam. The electron energy spectrum of this beam and the computed depth dose profile are close to those in Reference (18). The depth dose profile is substantially different (for annealing) than the beam used for pulse epitaxy.

The results are presented in Figure 4-2. The standard deviation of the sheet resistance after annealing is ±4 percent. Some of the peak variations, which are high on one side and low on the other, are traceable to a misalignment of the apparatus. The random variation, typical of pulsed electron beam processing, is less than ±4 percent. No point on the sample wafer has been left unannealed and no point has been damaged. This result is reproducible, and over 600 three-inch-diameter solar cells on a program for JPL[(20)] have been processed with this beam for annealing the junction implant. No further experiments to improve uniformity are planned at this time.

The wafer used to generate the data in Figure 4-2 will be used for helium ion backscatter measurements of junction depth. It is hoped that these measurements of sheet resistance can be correlated with junction depth or dopant substitutionality.

## 4.4 SOLID PHASE ANNEAL

The SPI-PULSE™ 600 is a small pulse line capable of producing up to 11 joules of output in one pulse at 100 kV charging. It is a reduced size version of the main pulse processor at Spire Corporation and has the advantage of greater reliability and high pulse repetition rate. For this latter capability it was selected as the initial processor for solid phase anneal experiments.

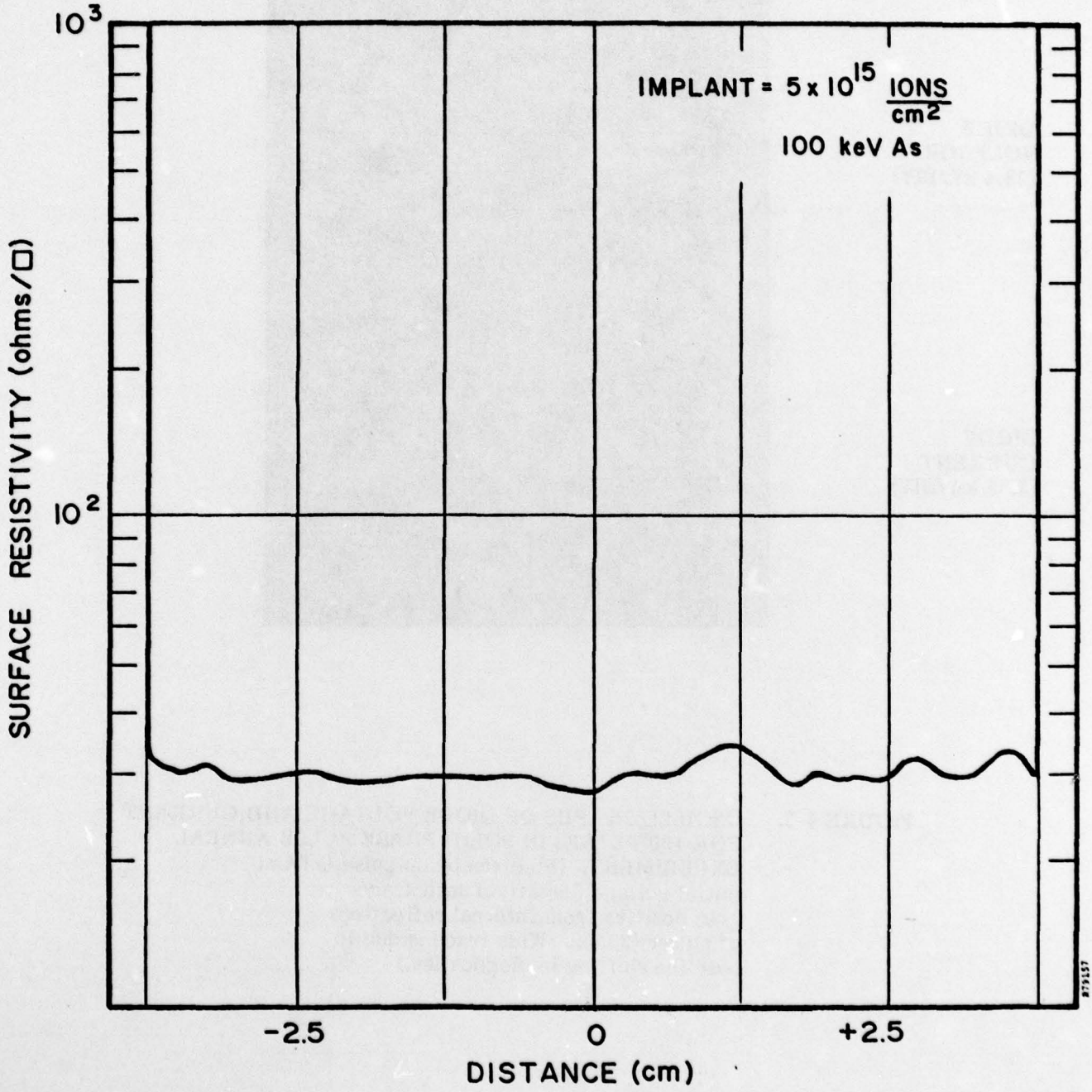



**FIGURE 4-2. SHEET RESISTANCE OF 3-inch WAFER AFTER ANNEALING BY ELECTRON BEAM IN ONE PULSE**

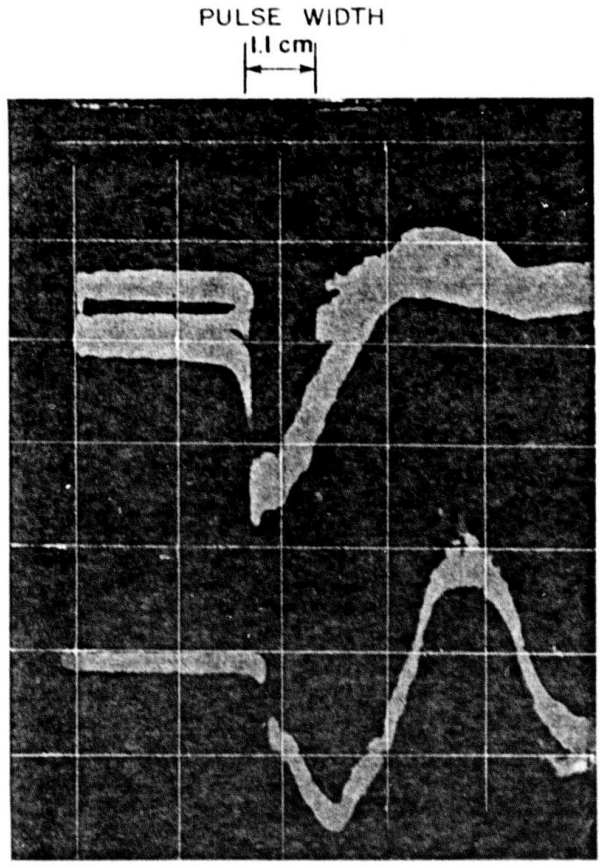



FIGURE 4-3. OSCILLOGRAPHS OF DIODE VOLTAGE AND CURRENT FOR 100 PULSES IN SOLID PHASE PULSE ANNEAL EXPERIMENT. (Electron beam pulse is from initial voltage (negative) until trace goes positive from internal reflections of pulser (35 ns). Wide trace is due to baseline shifting in diagnostics.)

The pulser was connected to a 155 kV, 5 mA power supply. For insulation purposes, it was restricted to 100 kV. The charge line was monitored and activated an automated trigger at about 1 pps. Typical, reproducible diode current and voltage traces are shown in Figure 4-3. The pulse width is much shorter, under 40 ns, than for earlier results. The average electron energy, the energy spectrum, and the deposition profile will be measured from this data in the next quarter.

Samples for these experiments were prepared by the ion implantation of 1 - 10 ohm-cm silicon with either 10 keV phosphorus to a dose of $2.5 \times 10^{15}/cm^2$ or 100 keV arsenic to a dose of $1 \times 10^{16}/cm^2$. Both implants are heavily damaging, leaving the surface amorphous. The first implant condition corresponds to Spire's experiments on pulse annealed solar cells and was used as a standard of comparison. The second implant was used for diagnostics (helium ion backscattering is planned).

Chronologically, the experiment was conducted by first trying to find a pattern of annealing in one pulse that was suitable, then reducing the fluence and testing for multiple pulse annealing. In this test, the easily visible change in color when amorphous material is changed to crystalline silicon was used as the principal diagnostic. In all tests on the larger SPI-PULSE$^{TM}$ 5000, this color change was associated with good annealing, by liquid phase regrowth, of the ion-implantation damage in one pulse. As it turned out, the change in color could occur with a change from amorphous to polycrystalline material. This was not suspected until the first samples were analyzed by RHEED.

After developing a beam with a reproducible signature, five samples were processed with 1, 3, 10, 30, and 100 shots each. The visible pattern grew radially with an increasing number of pulses. The pattern after one shot was very small or not visible at all. The sample with 100 pulses was quartered and one slice analyzed by SIMS (see Figure 4-4) and another by RHEED (see Figure 4-5). Note that the combined measurement could be accomplished by helium ion backscattering alone. These measurements show no redistribution of the dopant profile before and after pulsing — implying that the material was not melted. They also show that the amorphous, implanted surface was turned to polycrystalline silicon without epitaxy observed at the surface. Incomplete epitaxial regrowth may have occurred but was not observed by these diagnostic techniques.

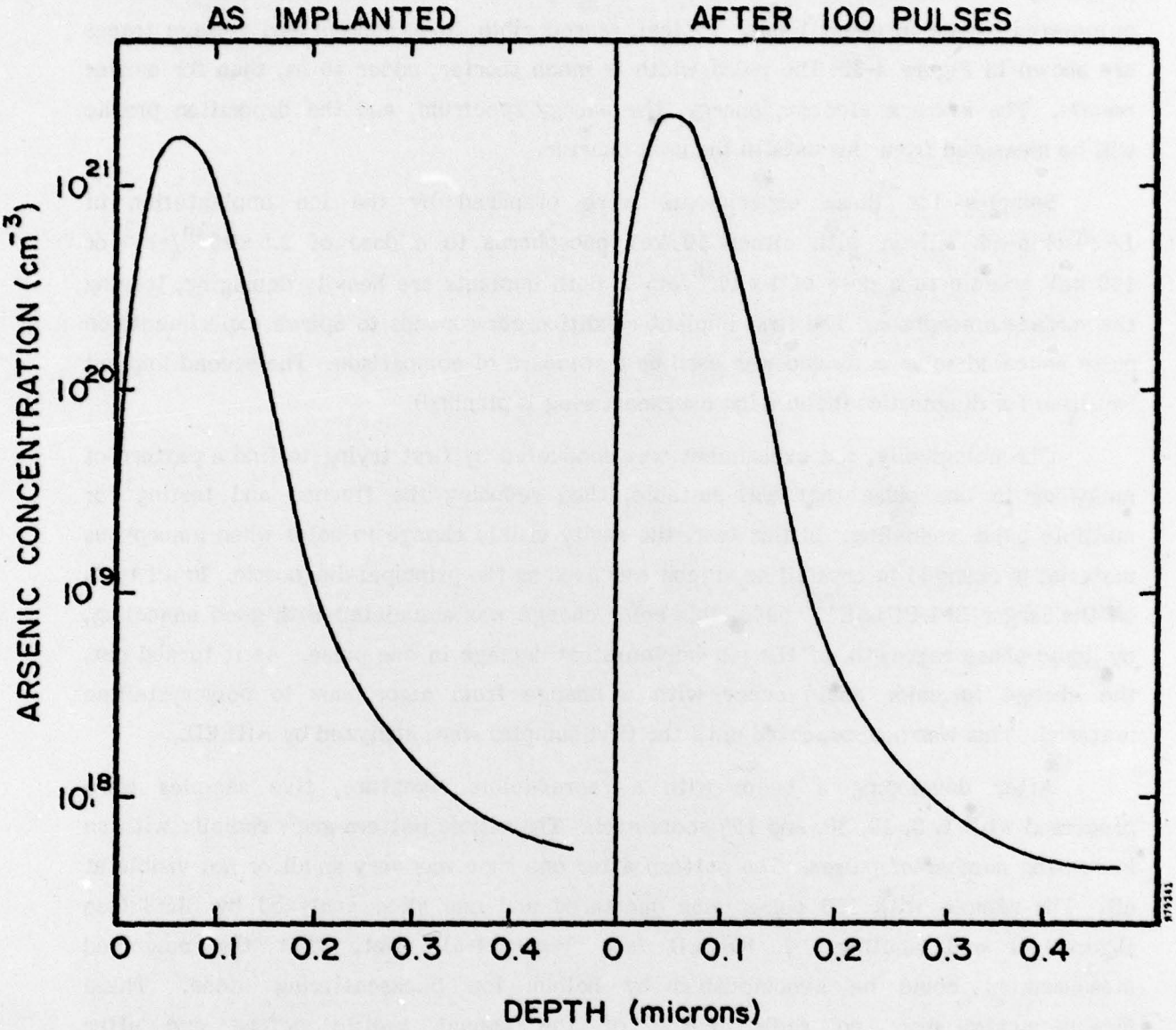



FIGURE 4-4. SIMS DATA FOR IMPLANTED ($10^{16}$/cm$^2$ 100 keV As) AND PULSE HEATED SILICON (BELOW MELT POINT). (Note: Depth scales not identical but curves are similar. Noise, shown averaged, due to single particle counting in detector.)

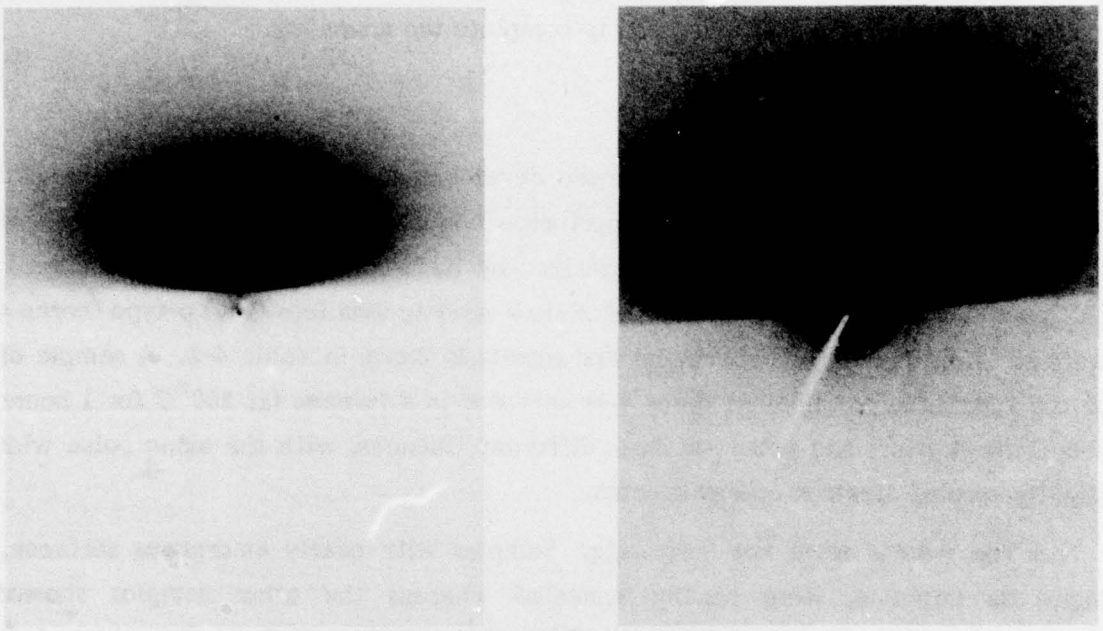



FIGURE 4-5. RHEED PATTERNS OF IMPLANTED SILICON
(a) WITH $10^{16}/cm^2$ 100 keV As IONS; AND
(b) AFTER 100 LOW FLUENCE PULSES, SHOWING POLYCRYSTALLINE SURFACE

Future plans are to extend the analysis so as to measure incomplete epitaxial regrowth of these samples, and to determine the rate of regrowth. Since melting was not observed, the fluence of the beam could be increased for faster regrowth per pulse, and/or the number of pulses increased to complete the annealing.

## 4.5 LIQUID PHASE ANNEALING

To identify the areas where more development of this technique is necessary, a preliminary comparison test was performed much ahead of the planned program schedule. The electron beam, characterized by Reference (18), was used to anneal $10^{12}$, $10^{13}$, $10^{14}$, and $10^{15}/cm^2$ implants of 25 keV arsenic ions into (100) p-type (boron doped) wafers. A matrix of the experiment and results is shown in Table 4-2. A sample of each of the four different implant doses was annealed in a furnace (at 550°C for 1 hours, then 850°C for 1 hour) and pulsed at four different fluences, with the same pulse width and slightly varying electron energy spectra.

The results were not surprising. Samples with nearly amorphous surfaces, from high-dose implants, were readily annealed whereas the other samples showed less activation of the implanted dopant. This contrast is caused by the reduced fluence required to melt an amorphous layer of silicon, which contains greater free energy than crystalline silicon and shows an exothermic reaction upon recrystallization[21]. Future tests with liquid phase annealing will examine the effect of higher fluence on low dose implants.

TABLE 4-2. LIQUID PHASE ANNEAL:
PRELIMINARY RESULTS

(Sheet Resistance Values in $\Omega/\square$ are listed in the matrix as a function of pulsed beam fluence and implant dose.)

| Fluence | 0.17 | 0.19 | 0.22 | 0.26 | Furnace |
|---|---|---|---|---|---|
| $10^{12}$ | 39.3 | 31.7 | 12.2 | 28.7 | 11.9 |
| $10^{13}$ | 113 | 62.4 | 120 | 141 | 38.8 |
| $10^{14}$ | 27.5 | 23.7 | 25.2 | 26.0 | 16.8 |
| $10^{15}$ | 19.6 | — | 13.7 | 15.6 | 14.8 |

Notes: Furnace Anneal: 2 hr @ 550°C, 1 hr @ 850°C
Implant: 25 keV $As^{75}$
Substrate: 1-2 ohm-cm (100)
Damage: All samples at 0.26 cal/cm$^2$
Normal Fluence: 0.22 cal/cm$^2$

# SECTION 5
# CONCLUSIONS - FUTURE RESEARCH

This section will outline the specific experiments now in progress or planned for the next 6 months to continue work on Task 1, 2, and 3. Experiments for film deposition and pulsed epitaxy will be discussed together.

## 5.1 PULSED EPITAXY

Pulsed epitaxy of deposited films was demonstrated. Good control of the doping and autodoping of low temperature deposited and recrystallized films was not demonstrated. Most of the effort in Task 1 and Task 2 will be directed to this problem.

The first experiment is outlined in Table 1-1. Three-inch o.d. wafers (FZ, (100), 1-ohm-cm, boron doped) will be used as substrates. Eight will be implanted with a high-dose of arsenic to simulate a buried layer. Half of the implanted wafers will be annealed in a furnace and half will be pulsed electron beam annealed by liquid phase epitaxy. A film of small grain polysilicon or amorphous silicon will be deposited by LPCVD on all of these substrates plus four nonimplanted wafers. This will give six types of samples to be used for pulsed epitaxy. Two additional wafers, implanted and unimplanted without films, will be saved for comparison. After pulsing, all intact films will be analyzed by SEM, RHEED, and C-V analysis. Further interesting samples will be selected for analysis by x-ray diffraction, SIMS or Auger electron spectroscopy (AES), and deep-level transient spectroscopy (DLTS). Additional experiments will deposit a film by LPCVD on highly doped (0.003-ohm-cm), (111) substrates. Also, an infrared reactor will be tested for lower temperature deposition. The object here is to determine what processing parameters doped the poly film in the first series of experiments.

As a comparison to LPCVD, and because it shows higher deposition rates and potentially greater capability, plasma ion deposition will be tested. Initial samples will use silicon substrates with half the surface oxidized (0.1 - 0.5 micron thick) and deposit a film over half the total surface. This will allow characterization of the deposit with and without oxide layers. Pulsed epitaxy over the unoxidized region will be tried. Additional substrates will be etched in the deposition chamber to remove all oxide on the substrate before depositing a film for testing pulse epitaxial regrowth. Films be analyzed by SEM, RHEED, and C-V analysis.

For thicker films, two experiments will be considered on a time available basis. One will use multiple layer pulsed epi techniques to show arbitrary thickness capability. The second will use thicker films from the plasma ion deposition experiment. The rate of deposition of fine grain or amorphous films by LPCVD is too slow for thick (over 1.0 micron) deposits. Possibly sputtered films will be used.

## 5.2 PULSE ANNEALING

Experiments will continue in two directions. The solid phase annealing experiment will be shifted to a different pulse generator for better control of the beam fluence and other processing variables, such as vacuum chamber pressure. Samples with low dose implants, about $10^{13}/cm^2$, will be used as well as high dose implants which makes the surface amorphous. Liquid phase annealing experiments will use higher fluences and test the annealing of other ion implants, especially boron. An experiment with multiple pulses in liquid phase annealing is being considered to determine the maximum depth of diffusion attainable this way.

## 5.3 ANALYSIS

Additional analytical techniques will be used to characterize samples in the future. The most urgent need is for a rapid survey technique to examine samples from the solid phase anneal experiment. Previously, C-V analysis using a mercury probe contact was tried, but it failed due to the polycrystalline material. Capacitance-voltage analysis can still be used with success indicating good material but failure indicating little. Optical observations are not reliable. A point probe measurement of photovoltaic response will be set up. This can qualitatively characterize annealed samples. Further, but limited, analysis by SIMS, RHEED, and helium ion backscattering are essential.

The next most useful technique to be used in the future is DLTS or transient capacitance spectroscopy, which can detect defects in crystalline material as a function of depth. It will be used to determine the electrical quality of pulsed epitaxy material short of making a series of devices. Additional analysis for impurities such as carbon and oxygen will also be undertaken during the next 6 months.

# SECTION 6
# SCHEDULE

The program schedule, as outlined in the optional program implementation plan, is shown in Figure 6-1. Work to date is about 2 months ahead of schedule. This has resulted in substantially more information available for this technical report than originally planned. It has also resulted in increased expenditures, as shown in Figure 6-2.

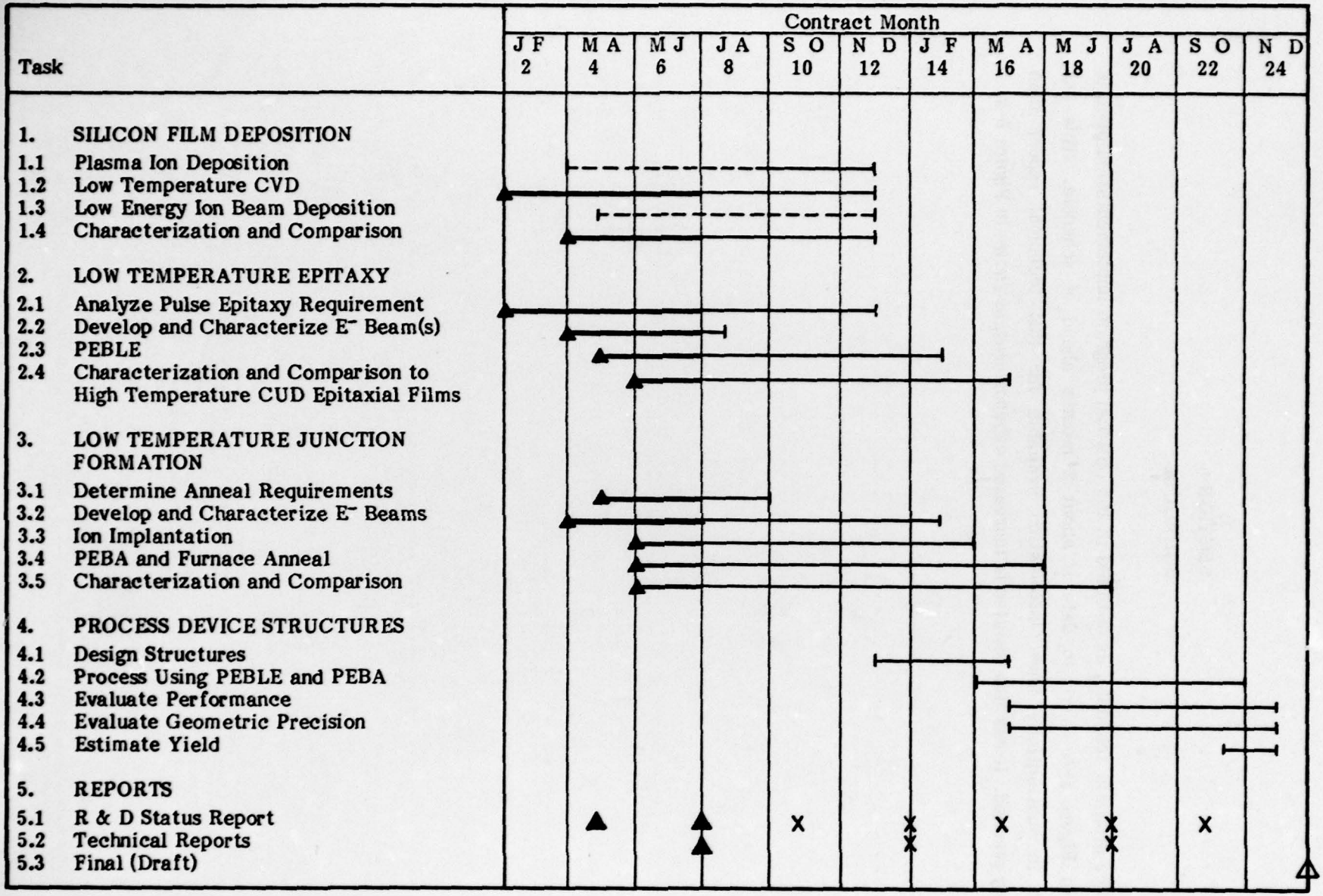



FIGURE 6-1. PROGRAM PLAN

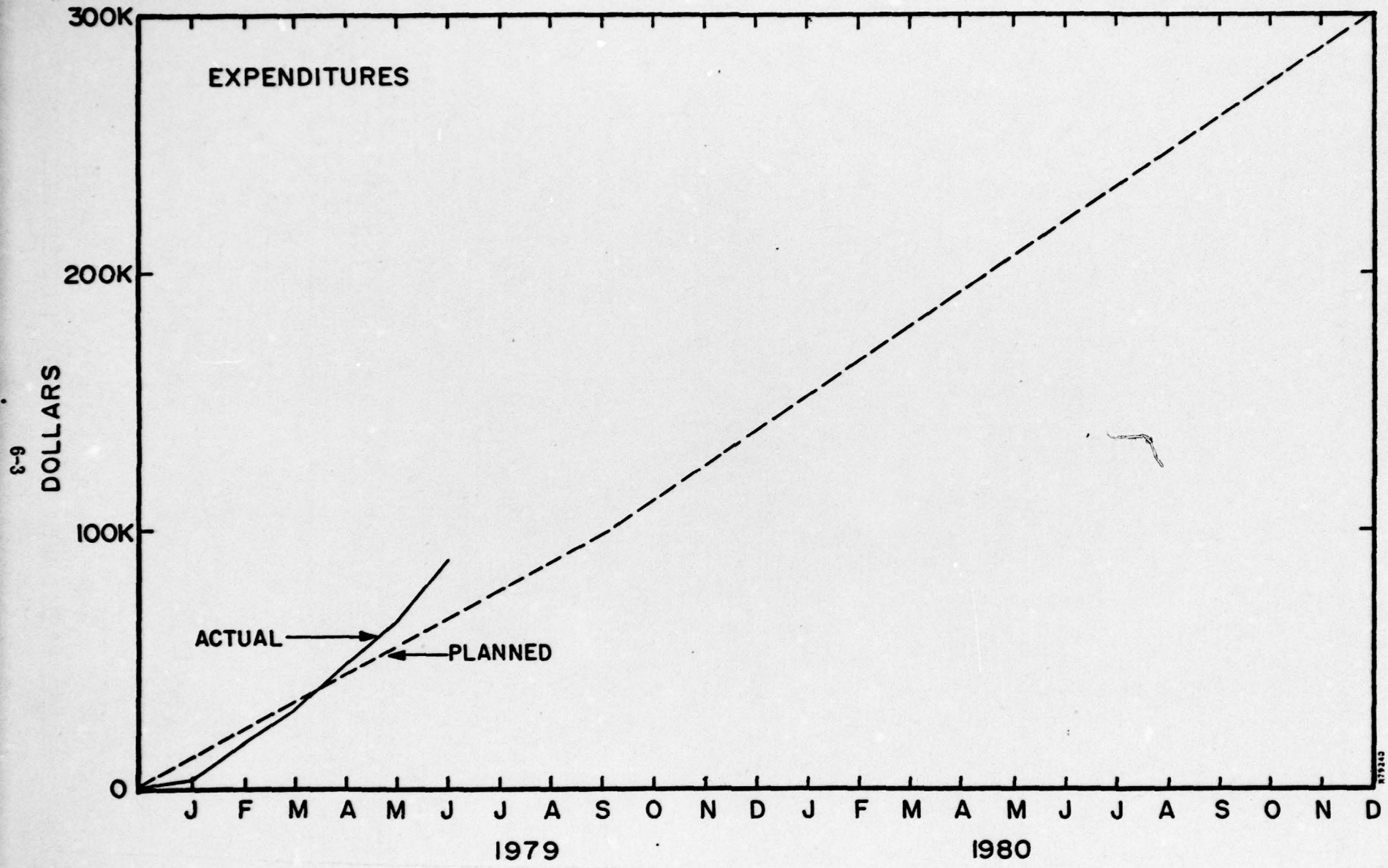



FIGURE 6-2. ACTUAL AND PLANNED EXPENDITURES

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